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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
STEPHANE POCAS, ET AL.	: EXAMINER: JONES, E.W.
SERIAL NO: 10/584,052	:
FILED: JUNE 22, 2006	: GROUP ART UNIT: 2892
FOR: METHOD OF SEALING TWO PLATES WITH THE FORMATION OF AN OHMIC CONTACT THERE BETWEEN	:

APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Appellants submit herewith their appeal of the final rejection presented in the Office Action dated February 1, 2011.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee, Commissariat A L'Energie Atomique.

II. RELATED APPEALS AND INTERFERENCES

Appellants' legal representatives and the assignee are aware of no appeals which will directly affect or be directly affected by or have any bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 27-29, 31-45, 53-57, and 65 stand rejected as noted below, and the rejections of Claims 27-29, 31-45, 53-57, and 65 are herein appealed A clean copy of pending Claims 27-29, 31-45, 53-57, and 65 are attached in the claims appendix. Claims 1-26, 30, 46-52, and 58-64 were previously canceled.

In the Office Action issued February 1, 2011, Claims 27-29, 34-36, 41-43, 45, 53, 54, and 65 were rejected under 35 U.S.C. §103(a) as unpatentable over Neilson et al. (U.S. Patent No. 6,054,369, hereinafter Neilson) in view of Kakumu (U.S. Patent No. 5,654,241) and further in view of Yamamoto et al. (U.S. Patent No. 4,577,396, hereinafter Yamamoto); Claims 31-33 and 55-57 were rejected under 35 U.S.C. §103(a) as unpatentable over Neilson, Kakumu, and Yamamoto, and further in view of Kish, Jr. et al. (U.S. Patent No. 5,783,477, hereinafter Kish) and Abe et al. (U.S. Patent Publication No. 2002/0157790, hereinafter Abe); Claims 37, 38, and 44 were rejected under 35 U.S.C. §103(a) as unpatentable over Neilson, Kakumu, and Yamamoto, and further in view of Kub et al. (U.S. Patent No. 6,274,892, hereinafter Kub); and Claims 39 and 40 were rejected under 35 U.S.C. §103(a) as

unpatentable over Neilson, Kakumu, and Yamamoto, and further in view Yu et al. (U.S. Patent No. 6,410,371, hereinafter Yu).

The Board of Appeals and Interferences has jurisdiction because the appealed Claims 27-29, 31-45, 53-57, and 65 have been twice rejected.

IV. STATUS OF THE AMENDMENTS

The Office Action issued February 1, 2011 is a final rejection. No amendment has been filed subsequent to this final rejection. All responses filed prior to February 1, 2011 were entered.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER[1]

Claim 27

The invention defined by Claim 27 describes a method of sealing a first wafer [Fig. 1A, element 2] and a second wafer [Fig. 1B, element 12] each made of semiconducting materials [spec., p. 6, ll. 28-31. The method comprises:

implanting a metallic species [Fig. 1A, element 4] in at least the first wafer [Fig. 1A, element 2] at a dose above 10^{16} species/cm^2 [spec., p. 8, ll. 5-15, p. 7, ll. 27-28, p. 2, ll. 24-25, and example 1-6 beginning at p. 12 of the spec.],

assembling the first wafer and the second wafer by molecular bonding [Fig. 1B, spec., p. 9, ll. 9-21], and

after the molecular bonding, forming a metallic ohmic contact including alloys formed between the implanted metallic species and the semiconducting materials of the first wafer and the second wafer, said metallic ohmic contact being formed at an assembly

[1] The Rules of Practice before the Board of Patent Appeals and Interference, 37 C.F.R. § 41.37(c)(v) requires that a concise explanation of the subject matter recited in each independent claim be provided with reference to the specification by page and line numbers and to the drawings by reference characters. However, Appellants' compliance with such requirements anywhere in this document should in no way be interpreted as limiting the scope of the invention recited in all pending claims, but simply as non-limiting examples thereof.

interface between the first wafer and the second wafer [Fig. 1C, spec., p. 3, lines 11-14, p. 10, l. 13 to p. 10, l. 30, p. 15, ll. 4-5],

wherein the forming includes causing the implanted metallic species to diffuse towards the interface between the first wafer with the second wafer and beyond the interface [Fig. 1C, spec., p. 10, l. 13 to p. 10, l. 30, p. 12, ll. 12-14, p. 13, ll. 6-12 and 26, p. 14, ll. 18-20].

Claim 53

The invention defined by Claim 53 describes a method of sealing a first wafer [Fig. 1A, element 2] and a second wafer [Fig. 1B, element 12] each made of semiconducting materials [spec., p. 6, ll. 28-31. The method comprises:

implanting a metallic species in at least the first wafer [Fig. 1B, element 2], at a depth of between 5 nm and 20 nm [spec, page 21, ll. 21-22] under a surface of said first wafer, at a dose above 10^{16} species/cm^2 [spec., p. 8, ll. 5-15, p. 7, ll. 27-28, p. 2, ll. 24-25, and example 1-6 beginning at p. 12 of the spec.],

assembling the first wafer and the second wafer by molecular bonding [Fig. 1B, spec., p. 9, ll. 9-21],

after the molecular bonding, forming a metallic ohmic contact including a silicide alloy formed between the implanted metallic species and the semiconducting materials of the first wafer and the second wafer, said metallic ohmic contact being formed at an assembly interface between the first wafer and the second wafer [Fig. 1C, spec., p. 3, lines 11-14, p. 10, l. 13 to p. 10, l. 30, p. 15, ll. 4-5],

wherein the forming includes causing the implanted metallic species to diffuse towards the interface between the first wafer with the second wafer and beyond the interface[Fig. 1C, spec., p. 10, l. 13 to p. 10, l. 30, p. 12, ll. 12-14, p. 13, ll. 6-12 and 26, p. 14, ll. 18-20].

Claim 65

The invention defined by Claim 65 describes a method of sealing a first wafer [Fig. 1A, element 2] and a second wafer [Fig. 1B, element 12] each made of semiconducting materials [spec., p. 6, ll. 28-31. The method comprises:

implanting a metallic species [Fig. 1A, element 4] in at least the first wafer [Fig. 1A, element 2] at a dose above 10^{16} species/cm^2 [spec., p. 8, ll. 5-15, p. 7, ll. 27-28, p. 2, ll. 24-25, and example 1-6 beginning at p. 12 of the spec.],

assembling the first wafer and the second wafer by molecular bonding, wherein the first wafer and the second wafer include silicon [Fig. 1B, spec., p. 9, ll. 9-21], and

after the molecular bonding, forming a metallic ohmic contact including a silicide alloy formed between the implanted metallic species and the semiconducting materials of the first wafer and the second wafer, said metallic ohmic contact being formed at an assembly interface between the first wafer and the second wafer [Fig. 1C, spec., p. 3, lines 11-14, p. 10, l. 13 to p. 10, l. 30, p. 15, ll. 4-5],

wherein the forming includes causing the implanted metallic species to diffuse towards the interface between the first wafer with the second wafer and beyond the interface[Fig. 1C, spec., p. 10, l. 13 to p. 10, l. 30, p. 12, ll. 12-14, p. 13, ll. 6-12 and 26, p. 14, ll. 18-20].

VI. GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

Whether Claims 27-29, 34-36, 41-43, 45, 53, 54, and 65 are unpatentable under 35 U.S.C. §103(a) as obvious over Neilson in view of Kakumu, and further in view of Yamamoto.

Whether Claims 31-33 and 55-57 are unpatentable under 35 U.S.C. §103(a) as obvious over Neilson, Kakumu, and Yamamoto, and further in view of Kish and Abe.

Whether Claims 37, 38, and 44 are unpatentable under 35 U.S.C. §103(a) as obvious over Neilson, Kakumu, and Yamamoto, and further in view of Kub.

Whether Claims 39 and 40 are unpatentable under 35 U.S.C. §103(a) as obvious over Neilson, Kakumu, and Yamamoto, and further in view Yu.

VII. ARGUMENT

A. The rejections of Claims 27, 53, and 65 are incorrect

The Examiner's rejections are based on improper hindsight reconstruction. The reasoning offered by the Examiner as to why a person of ordinary skill in the art would supposedly modify the primary reference Neilson is speculative, unsupported by substantial evidence, and lacks any consideration as to how such proposed modifications would affect the device of Nielson.

i. Differences between Claims 27, 53, and 65 and Nielson

Exemplary Claim 27 recites:

> implanting a metallic species in at least the first wafer at a dose above 10^{16} species/cm^2,
>
> assembling the first wafer and the second wafer by molecular bonding, and
>
> after the molecular bonding, forming a metallic ohmic contact including alloys formed between the implanted metallic species and the semiconducting materials of the first wafer and the second wafer, said metallic ohmic contact being formed at an assembly interface between the first wafer and the second wafer,
>
> wherein the forming includes causing the implanted metallic species to diffuse towards the interface between the first wafer with the second wafer and beyond the interface.

Claim 65 recites similar features, except Claim 65 specifies that the ohmic contact includes a silicide alloy. Claim 53 recites similar features, except Claim 53 specifies the implantation depth.

Neilson is concerned with the switching speed of transistors.[2] Recombination centers are locations of crystallographic strain.[3] The purpose of Neilson to is to provide "recombination centers of a semiconductor device [that] are concentrated in a buffer layer or near a wafer-to-wafer bonding interface."[4] Neilson also identifies that another purpose is to provide a semiconductor device in which the density of recombination centers in a buffer layer adjacent to a blocking layer is significantly higher than that of the blocking layer.[5] The density of the recombination centers may be controlled by doping one or both of the bonding surfaces with a suitable dopant or dopants.[6]

In Neilson, the concentration of 10^{14} cm^{-3} to 10^{19} cm^{-3} (col.4, l.51 of Neilson) is far too low to make an ohmic contact (see Sze, page 187, first sentence of §3.6: "An ohmic contact is defined as a metal-semiconductor contact that has a negligible junction resistance relative to the total resistance of the semiconductor device" [emphasis added]). It is important to appreciate that Neilson's units are **cm^{-3}**, while the claim recites **cm^{-2}** (note the difference in exponents). Thus, the claimed 10^{16} species/cm^2 is **not** within the range of 10^{14} cm^{-3} to 10^{19} cm^{-3} described in Neilson.

With the concentrations given in Neilson, recombination centers are made, and any reaction between the dopants and the substrate is too insignificant to form an ohmic contact. Using software called SRIM, the doses of implanted species of Neilson have been calculated based on the concentration indicated in col.4, l.51 of Neilson:

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[2] Neilson, col. 1, lines 10-23.
[3] Neilson, col. 1, lines 26-29.
[4] Neilson, col. 2, lines 43-45.
[5] Neilson, col. 2, lines 46-50.
[6] Neilson, col. 4, lines 36-38.

- For a concentration of $10^{19}/cm^{-3}$ a dose of $1.3 \times 10^{13}/cm^2$ at 10 keV and $2.10^{14}/cm^2$ at 250 keV are obtained.
- For a concentration of $10^{14}/cm^{-3}$ a dose of $2.10^{14}/cm^2$ at 10 keV and $2.10^{9}/cm^2$ at 250 keV are obtained.

The doses employed in Neilson are therefore much lower than the claimed at least $10^{16}/cm^2$. Col. 4, ll. 57-59 of Neilson states "the dopant may be selected to provide optimum switching performance (if this is desired) without regard for its solubility or diffusion coefficient." The "without regard for its solubility or diffusion coefficient" is in agreement with a very low concentration, very far from saturation where solubility is not yet a problem. **The Examiner fails to make any findings of fact, supported by substantial evidence, to support a contrary position.**

Furthermore, Neilson fails to disclose the claimed "wherein the forming includes causing the implanted metallic species to diffuse towards the interface between the first wafer with the second wafer and beyond the interface." As explained at col. 4, ll. 46-49 of Neilson, a high temperature treatment is "to distribute the dopants in what will become buffer layer 24 and establish the desired concentration." There is no disclosure that the dopants diffuse beyond the interface (i.e., the interface between elements 22 and 24 of Neilson).

Thus, Neilson at least differs from Claims 27, 53, and 65 in the doping concentration used, the formation of an ohmic contact at an assembly interface between the first wafer and the second wafer,[7] and that the forming includes causing the implanted metallic species to diffuse towards the interface between the first wafer with the second wafer and beyond the interface.

ii. A person of ordinary skill in the art would not modify Neilson to include an ohmic contact at the interface of bonding surfaces

[7] See, for example, pp. 3-4 of the Office Action issued February 1, 2011.

The purpose of Neilson is to form recombination centers.[8] Elimination of the recombination centers would render Neilson unsatisfactory for its intended purpose (see, col. 2, line 40 to col. 3, line 27 of Neilson). According to MPEP §2143.01(V), "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." MPEP §2143.01(VI) also states, "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious."

Changing the recombination centers to an ohmic contact would change the principle of operation of the device of Neilson since the recombination centers are an integral part of the semiconductor device of Neilson. The dopants would be concentrated in the ohmic contact because they have a low density in the material. No recombination centers would remain to provide the needed "layer adjacent a blocking layer of a semiconductor device is provided with a significantly higher density of recombination centers."[9] There is **no evidence** to support a position that Neilson includes or should include both recombination centers and an ohmic contact formed at an assembly interface between the first wafer and the second wafer.

Appellants respectfully submit that a person of ordinary skill in the art would not modify Neilson to have both recombination centers and an ohmic contact. Neilson states "a layer adjacent a blocking layer of a semiconductor device is provided with a significantly higher density of recombination centers."[10] To the extent it is even possible to modify Neilson so that some of the recombination centers are changed into an ohmic contact, such a

[8] Neilson, col. 2, lines 40-57.
[9] Neilson, col. 1, lines 5-10. See also, Neilson, col. 2, lines 46-50.
[10] Neilson, col. 1, lines 5-10. See also, Neilson, col. 2, lines 46-50.

modification would frustrate the above-noted purpose of Neilson as it would alter the density of the recombination centers. In addition, col. 2, lines 51-57 of Neilson describes that recombination centers are substantially absent from the blocking layer. Thus, there is no reason to have recombination centers or an ohmic contact at the blocking layer.

Neilson describes transistors.[11] It does not make sense to form an ohmic contact at the blocking layer and/or buffer layer of Neilson. Neilson concerns an interface between NP regions of a transistor (see Figs. 2C or 2D) or an interface with a blocking layer (see Figs. 2A or 1D). A person of ordinary skill in the art would not form an ohmic contact at an interface with a blocking layer which, roughly speaking, aims to block charge circulation. Col. 1, lines 59 to col. 2, line 19 of Neilson describes that the blocking layer has a high resistance, which is contradictory with having an ohmic contact. Ohmic contacts are not built where resistivity is to be kept high. The blocking layer is also for having a low leakage current (see, col. 1, line 61 of Neilson), which again is contradictory with having an ohmic contact at the interface with the blocking layer.

What is important in Neilson in selecting a dopant is **not** its ability to react with the substrate. Rather, Neilson is concerned with the energy levels (see, col. 5, lines 5-7 in combination with col. 1, lines 31-36 of Neilson). If the dopants of Neilson were suppose to react with the substrate, the energy levels of the dopants would be totally different and their ability to form recombination centers would be lost. See, also, claim 26 of Neilson stating "selecting a dopant for the doping step based on an energy level of the dopant." Thus, Neilson does not disclose "forming a metallic ohmic contact including alloys formed between the implanted metallic species and the semiconducting materials of the first wafer and the second wafer."

[11] Neilson, col. 1, lines 11-22.

With respect to combining prior art elements, Appellants refer to the recently issued Examination Guidelines Update: Developments in the Obviousness Inquiry After KSR v. Teleflex (hereinafter Obviousness Guidelines).[12] These guidelines state:

> Even though the components are known, the combining step is technically feasible, and the result is predictable, the claimed invention may nevertheless be nonobvious when the combining step involves such additional effort that no one of ordinary skill would have undertaken it without a recognized reason to do so.[13]

The prior art does not recognize a problem with the device of Neilson. There is no recognized reason as to why a person of ordinary skill in the art would modify Neilson to include any extra steps or processing to form an ohmic contact as specified by the independent claims. In other words, the record does not include evidence as to why a person of ordinary skill in the art would dispose an ohmic contact at the buffer layer/blocking layer interface of a transistor. There is no evidence that this would increase the speed of the transistor or provide any other benefit to a transistor. Any such conclusion is mere speculation.

The PTO cannot base rejections on assumptions instead of established facts. See In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967) as follows:

> A rejection based on section 103 clearly must rest on a factual basis, and these facts must be interpreted without hindsight reconstruction of the invention from the prior art. In making this evaluation, all facts must be considered. The Patent Office has the initial duty of supplying the factual basis for its rejection. ***It may not, because it may doubt that the invention is patentable, resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in its factual basis*** (emphasis added).

iii. Examiner's cited evidence does not support his position

[12] Federal Register, Vol. 75, No. 169, September 1, 2010.
[13] Obviousness Guidelines, part A, combining prior art elements.

The Examiner cites four additional references as evidence at pp. 16-17 of the Office Action issued February 1, 2011.[14] The Examiner's evidence supposedly supports a conclusion that "the recombination centers 20 formed in buffer layer 24 in FIGS. 2a-d would still function as recombination centers if an ohmic contact is formed."[15] However, the Examiner does not make sufficient factual findings to support the above-noted position. The Examiner only characterizes these references as describing recombination centers, forming recombination centers, forming nickel silicide, or forming cobalt silicide. There are no findings of fact that any of these additional references teach that a transistor, such as the transistor of Nielson, would have recombination centers that provided the stated goals and purposes of Nielson if an ohmic contact is formed. The Examiner makes no factual findings regarding whether the references discussed at pp. 16-17 of the Action mailed February 1, 2011 would still have recombination centers if they are modified to form ***an ohmic contact***. The Examiner fails to identify a single one of these additional references as providing a teaching of ***both*** recombination centers and an ohmic contact being in a transistor. This is nothing more than an attempt to bring in isolated teachings into Neilson's device which amounts to improperly picking and choosing features from different references without regard to the teachings of the references as a whole.[16] See also In re Bergel, 130 USPQ 206, 208 (CCPA 1961)("The mere fact that it is *possible* to find two isolated disclosures that might be combined in such a way to produce the [invention] does not necessarily render such production obvious unless the art also contains something to suggest the desirability of the proposed combination."). The Examiner has identified nothing within the art of record which

[14] These references, along with the Sze refrence, are included in the evidence appendix of this brief.
[15] Office Action issued February 1, 2011, p. 16.
[16] See In re Ehrreich 590 F2d 902, 200 USPQ 504 (CCPA, 1979) (stating that patentability must be addressed "in terms of what would have been obvious to one of ordinary skill in the art at the time the invention was made in view of the sum of all the relevant teachings in the art, not in view of first one and then another of the isolated teachings in the art," and that one "must consider the entirety of the disclosure made by the references, and avoid combining them indiscriminately.")

would direct a person skilled in the pertinent art to make the selections necessary to have both recombination centers and an ohmic contact in the transistor of Neilson.

iv. Kakumu does not cure the deficiencies of Neilson

One of ordinary skill in that art would not find it obvious to pick and choose the doping concentration disclosed by Kakumu in order to use it instead of the doping concentration of Neilson.[17] There is no evidence that a person of ordinary skill in the art would have recognized any problem with the doping concentration of Neilson, nor would a person of ordinary skill in the art have any desire to reduce or eliminate the amount of recombination centers in the device of Neilson. Thus, there is no rationale for such a modification, absent improper hindsight based on the present claims.

While Kakumu may provide a reason for using its doping concentration to form titanium-silicide layers on portions where the source and drain are formed in a transistor,[18] Kakumu fails to explain why a person of ordinary skill in the art would find it obvious to incorporate such a feature to form an ohmic contact at an interface between a blocking layer and a buffer layer of a transistor such as the one disclosed in Neilson.

Page 3 of the Office Action issued February 1, 2011, with respect to combining Kakumu with Nielson, states "Kakumu discloses...implanting metallic species...at a dose above 10^{16} species/cm^2... to form reduced areas of resistance for ohmic contacts." The Examiner goes on to state that it would be obvious to use this feature in Neilson "to form areas of reduced resistance to carrier flow." However, there is no finding of fact, supported by substantial evidence, that Neilson requires reduced resistance to carrier flow. On the contrary, col. 2, l. 12 of Neilson makes it clear that the resistivity of the blocking layer is

[17] See In re Ehrreich 590 F2d 902, 200 USPQ 504 (CCPA, 1979) (stating that patentability must be addressed "in terms of what would have been obvious to one of ordinary skill in the art at the time the invention was made in view of the sum of all the relevant teachings in the art, not in view of first one and then another of the isolated teachings in the art," and that one "must consider the entirety of the disclosure made by the references, and avoid combining them indiscriminately.")
[18] Kakumu, col. 3, lines 35-38.

increased. Adding an ohmic contact as suggested by the Examiner would have the opposite effect than what is taught by Neilson (i.e., lower the resistivity).

Moreover, the difference between the doping concentration of Neilson and that of Kakumu is significant (i.e., an order of magnitude). The Examiner has failed to provide any explanation regarding why Kakumu's doping concentration, if used in the embodiments discussed in Neilson, would predictably provide for the same results. Col. 4, ll. 57-59 of Neilson states "the dopant may be selected to provide optimum switching performance (if this is desired) without regard for its solubility or diffusion coefficient." The "without regard for its solubility or diffusion coefficient" is in agreement with a very low concentration, very far from saturation where solubility is not yet a problem. Neilson's solubility is too low to form an ohmic contact. There is no evidence that a person of ordinary skill in the art would alter or modify Neilson to implant a substrate above the limit of solubility to achieve an ohmic contact. Such a change would alter the nature of Neilson's device by changing the device from a transistor to an electrical contact.[19] Further, such a modification to Neilson would render Neilson's device unsatisfactory for its intended purpose (i.e., it would no longer be a transistor).[20]

Furthermore, in Kakumu, the doped regions 18 cannot be at an interface between two substrates because of elements 13 and 16 (Fig. 2D of Kakumu) or elements 16, 27, and 28 (Fig. 2G of Kakumu) materially prevent a second substrate from being brought in contact with substrate 10. A person of ordinary skill in the art would not appreciate that techniques from Kakumu would form an ohmic contact "at an assembly interface between the first wafer and the second wafer." Thus, a proper combination of Neilson and Kakumu does not lead to the claimed invention.

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[19] See In re Ratti, 270 F.2d 810, 813, 123 USPQ 349, 352 (CCPA 1959) (reversing an obviousness rejection where the "suggested combination of references would require a substantial reconstruction and redesign of the elements shown in [the primary reference] as well as a change in the basic principle under which the [primary reference] construction was designed to operate.")
[20] See MPEP 2143.01-V.

v. Yamamoto does not cure the deficiencies of Neilson

While Yamamoto may provide a reason for forming a silicide "into a desired ***surface region*** of a silicon substrate" in its device,[21] Yamamoto fails to explain why a person of ordinary skill in the art would find it obvious to incorporate such a feature to form an ohmic contact at an interface between a blocking layer and a buffer layer of a transistor such as the one disclosed in Neilson. Moreover, it is not the silicide in Yamamoto that makes an ohmic contact. Rather, it is electrode material (see, col. 3, ll. 14-23 of Yamamoto stating "and ohmic contact can be formed with the Si substrate when the metal...and after the heat treatment...the electrode and wiring made of W, Mo, or Al are formed ***on*** the resulting silicide or alloy layer" (emphasis added)). Thus, Yamamoto does not teach "forming a metallic ohmic contact including alloys formed between the implanted metallic species and the semiconducting materials of the first wafer and the second wafer."

Page 4 of the Office Action issued February 1, 2011 states that Yamamoto is combined with Neilson "to form alloyed or sillicide areas of reduced resistance." This is contrary to the teachings of Neilson as noted above, wherein Neilson teaches that the resistivity of the blocking layer is increased.

In view of the above-noted distinctions, a proper combination of Nielson, Kakamu, and Yamamoto does not disclose every feature of independent Claims 27 and 65. Thus, a proper combination of Nielson, Kakamu, and Yamamoto does not render Claims 27-29, 31-45, 53-57, and 65 obvious.

vi. Kakumu and Yamamoto fail to teach the claimed "wherein the forming includes causing the implanted metallic species to diffuse towards the interface between the first wafer with the second wafer and beyond the interface"

As explained above, the Examiner's finding that Neilson teaches the claimed "wherein the forming includes causing the implanted metallic species to diffuse towards the

[21] Yamamoto, col. 2, lines 25-30, emphasis added.

interface between the first wafer with the second wafer and beyond the interface" is incorrect. Kakumu and Kamamoto fail to teach the claimed "wherein the forming includes causing the implanted metallic species to diffuse towards the interface between the first wafer with the second wafer and beyond the interface."

B. The rejection of Claims 31-33 and 55-57 as unpatentable over Neilson, Kakumu, and Yamamoto, and further in view of Kish and Abe is incorrect

Claims 31-33 and 55-57 depend from Claim 27 or 53, and are patentable for at least the reasons stated above.

C. The rejection of Claims 37, 38, and 44 as unpatentable over Neilson, Kakumu, and Yamamoto, and further in view of Kub is incorrect

Claims 37, 38, and 44 depend from Claim 27, and are patentable for at least the reasons stated above.

D. The rejection of Claims 39 and 40 as unpatentable over Neilson, Kakumu, and Yamamoto, and further in view Yu is incorrect

Claims 39 and 40 depend from Claim 27, and are patentable for at least the reasons stated above.

E. Conclusion

In view of the foregoing, it is respectfully submitted that the outstanding rejections are improper, not supported by substantial evidence, and must be reversed.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

Claims 1-26 (Canceled).

Claim 27 (Rejected). A method of sealing a first wafer and a second wafer each made of semiconducting materials, comprising:

implanting a metallic species in at least the first wafer at a dose above 10^{16} species/cm^2,

assembling the first wafer and the second wafer by molecular bonding, and

after the molecular bonding, forming a metallic ohmic contact including alloys formed between the implanted metallic species and the semiconducting materials of the first wafer and the second wafer, said metallic ohmic contact being formed at an assembly interface between the first wafer and the second wafer,

wherein the forming includes causing the implanted metallic species to diffuse towards the interface between the first wafer with the second wafer and beyond the interface.

Claim 28 (Rejected). The method according to claim 27, wherein the forming includes applying a heat treatment at a temperature equal at least to a formation temperature of the said alloys .

Claim 29 (Rejected). The method according to claim 27, wherein the implanting includes implanting the metallic species at a depth of between 5 nm and 20 nm under a surface of the first wafer.

Claim 30 (Canceled).

Claim 31 (Rejected). The method according to claim 27, further comprising:

processing the first wafer to make all or part of a surface layer of the first wafer amorphous.

Claim 32 (Rejected). The method according to claim 31, wherein the processing includes depositing an amorphous material layer before and/or after implantation of the metallic species.

Claim 33 (Rejected). The method according to claim 31, wherein the processing includes implanting hydrogen.

Claim 34 (Rejected). The method according to claim 27, wherein the first wafer and the second wafer are made from a material chosen from among silicon, gallium arsenide (GaAs), SiC (silicon carbide), InP (Indium phosphide), Germanium (Ge), or silicon-Germanium (SiGe).

Claim 35 (Rejected). The method according to claim 27, wherein the implanted species includes one or more of Nickel, palladium, Cobalt, Platinum, Tantalum, Tungsten, Titanium, or Copper.

Claim 36 (Rejected). The method according to claim 27, wherein at least one of the wafers is a heterostructure.

Claim 37 (Rejected). The method according to claim 27, further comprising:

thinning at least one of the wafers after the assembling or after the forming of the metallic compounds.

Claim 38 (Rejected). The method according to claim 27, wherein at least one of the wafers is a debondable structure.

Claim 39 (Rejected). The method according to claim 27, wherein at least one of the wafers includes a weakening plane.

Claim 40 (Rejected). The method according to claim 39, further comprising:

thinning the wafer including the weakening plane d by fracture along said weakening plane, after the assembling or after the forming of the metallic compounds.

Claim 41 (Rejected). The method according to claim 27, wherein at least one of the wafers includes at least one circuit or circuit layer.

Claim 42 (Rejected). The method according to claim 27, wherein the implanting includes using a mask to obtain local implantation zones.

Claim 43 (Rejected). The method according to claim 27, further comprising:

forming an insulating layer on the first wafer, before the implanting.

Claim 44 (Rejected). The method according to claim 27, further comprising:

thinning the first wafer after implantation of the metallic species.

Claim 45 (Rejected). The method according to claim 27, wherein the first wafer includes at least one insulating zone located at a surface so as to obtain local implantation zones.

Claims 46-52 (Canceled).

Claim 53 (Rejected). A method of sealing a first wafer and a second wafer each made of semiconducting materials, comprising:

implanting a metallic species in at least the first wafer, at a depth of between 5 nm and 20 nm under a surface of said first wafer, at a dose above 10^{16} species/cm^2,

assembling the first wafer and the second wafer by molecular bonding,

after the molecular bonding, forming a metallic ohmic contact including alloys formed between the implanted metallic species and the semiconducting materials of the first wafer and the second wafer, said metallic ohmic contact being disposed at an assembly interface between the first wafer and the second wafer,

wherein the forming includes causing the implanted metallic species to diffuse towards the interface between the first wafer with the second wafer and beyond the interface.

Claim 54 (Rejected). The method according to claim 53, wherein the forming includes applying a heat treatment at a temperature equal at least to a formation temperature of the said metallic compounds.

Claim 55 (Rejected). The method according to claim 53, further comprising:

processing the first wafer to make all or part of a surface layer of the first wafer amorphous.

Claim 56 (Rejected). The method according to claim 55, wherein the processing further comprises depositing an amorphous material layer before and/or after implantation of the metallic species.

Claim 57 (Rejected). The method according to claim 55, wherein the processing includes implanting hydrogen.

Claim 58 (Rejected): A structure obtained by the method of claim 27, wherein the metallic compounds include at least one metal chosen from among nickel, palladium, cobalt, platinum, tantalum, titanium, or copper.

Claim 59 (Rejected): The structure according to claim 58, wherein the semiconducting materials are selected from among Si, GaAs, SiC, InP, or SiGe.

Claim 60 (Rejected): The structure according to claim 58, wherein at least one of the substrates is a heterostructure.

Claim 61 (Rejected): The structure according to claim 58, wherein at least one of the substrates is a thin film.

Claim 62 (Rejected): The structure according to claim 58, wherein at least one of the substrates includes one or more of electronic, optical, or mechanical components.

Claim 63 (Rejected): The structure according to claim 58, wherein one of the substrates is a thin film made of silicon comprising RF circuits.

Claim 64 (Rejected): The structure according to claim 63, wherein the other substrate is made of high resistivity silicon.

Claim 65 (Rejected). A method of sealing a first wafer and a second wafer each made of semiconducting materials, comprising:

implanting a metallic species in at least the first wafer at a dose above 10^{16} species/cm^2,

assembling the first wafer and the second wafer by molecular bonding, wherein the first wafer and the second wafer include silicon, and

after the molecular bonding, forming a metallic ohmic contact including a silicide alloy formed between the implanted metallic species and the semiconducting materials of the first wafer and the second wafer, said metallic ohmic contact being formed at an assembly interface between the first wafer and the second wafer,

wherein the forming includes causing the implanted metallic species to diffuse towards the interface between the first wafer with the second wafer and beyond the interface.

IX. EVIDENCE APPENDIX

Narayan et al. (U.S. Patent 4,181,538)

Francis et al. (U.S. Patent Publication 2003/0057522)

Oostra et al. (U.S. Patent No. 5,354,697)

Van Ommen et al. (U.S. Patent No. 5,236,572)

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United States Patent [19]

Narayan et al.

[11] **4,181,538**

[45] **Jan. 1, 1980**

[54] **METHOD FOR MAKING DEFECT-FREE ZONE BY LASER-ANNEALING OF DOPED SILICON**

[75] Inventors: **Jagdish Narayan**, Knoxville; **Clark W. White**, Oak Ridge; **Rosa T. Young**, Knoxville, all of Tenn.

[73] Assignee: **The United States of America as represented by the United States Department of Energy**, Washington, D.C.

[21] Appl. No.: **945,925**

[22] Filed: **Sep. 26, 1978**

[51] **Int. Cl.**[2] **H01L 21/26**; H01L 21/268

[52] **U.S. Cl.** ..... **148/1.5**; 148/187; 219/121 L; 357/91

[58] **Field of Search** ..... 148/1.5, 187; 357/18, 357/91; 219/121 L

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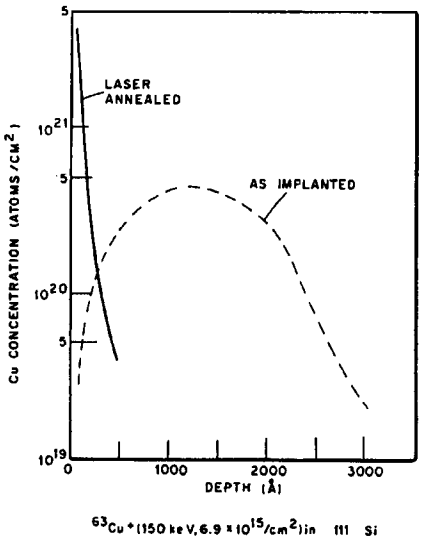
Primary Examiner—L. Dewayne Rutledge
Assistant Examiner—Upendra Roy
Attorney, Agent, or Firm—R. V. Lupo; Stephen D. Hamel; Fred O. Lewis

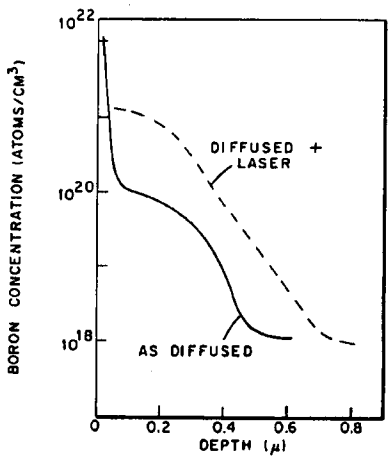
[57] **ABSTRACT**

This invention is a method for improving the electrical properties of silicon semiconductor material. The method comprises irradiating a selected surface layer of the semiconductor material with high-power laser pulses characterized by a special combination of wavelength, energy level, and duration. The combination effects melting of the layer without degrading electrical properties, such as minority-carrier diffusion length. The method is applicable to improving the electrical properties of n- and p-type silicon which is to be doped to form an electrical junction therein. Another important application of the method is the virtually complete removal of doping-induced defects from ion-implanted or diffusion-doped silicon substrates.

9 Claims, 13 Drawing Figures



$^{63}Cu^{+}$(150 keV, $6.9 \times 10^{15}/cm^2$)in 111 Si



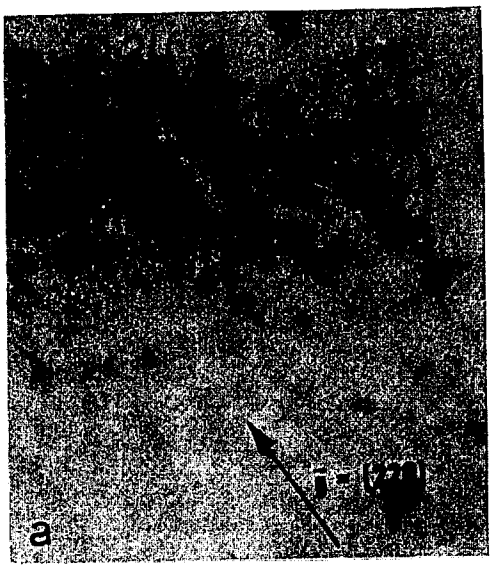


Fig. 1a

Fig. 1b

Fig. 2

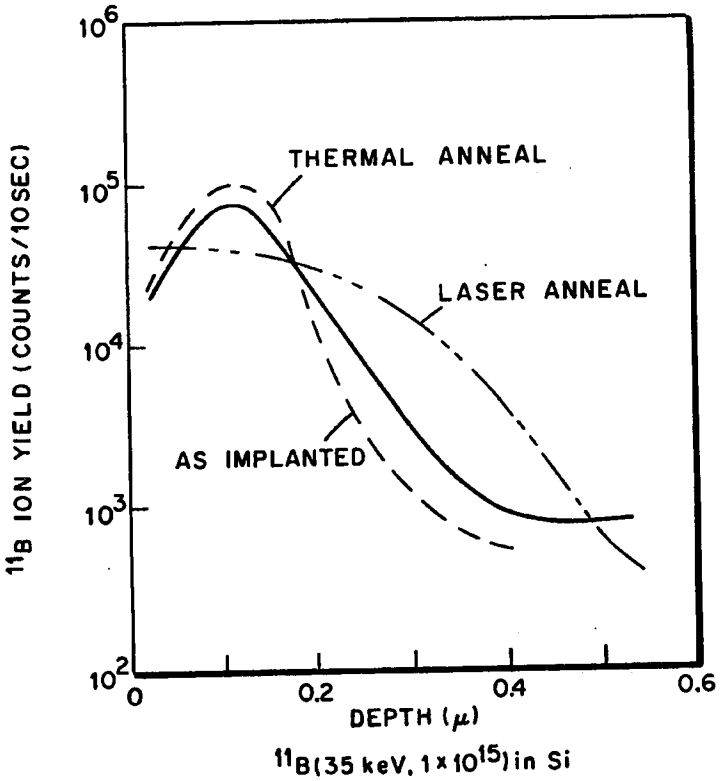

10^6
10^5
10^4
10^3
10^2
^{11}B ION YIELD (COUNTS/10SEC)
THERMAL ANNEAL
LASER ANNEAL
AS IMPLANTED
0
0.2
0.4
0.6
DEPTH (μ)
^{11}B(35 keV, 1×10^{15}) in Si

Fig. 4

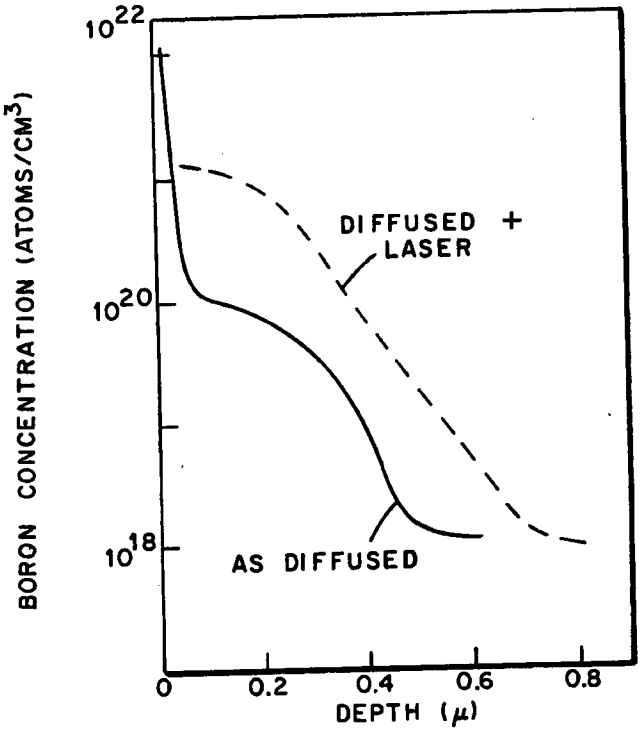

10^{22}
10^{20}
10^{18}
BORON CONCENTRATION (ATOMS/CM^3)
DIFFUSED + LASER
AS DIFFUSED
0
0.2
0.4
0.6
0.8
DEPTH (μ)

Fig. 3a

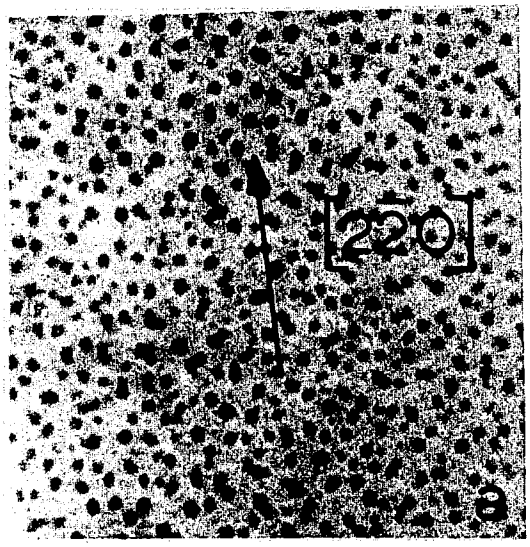
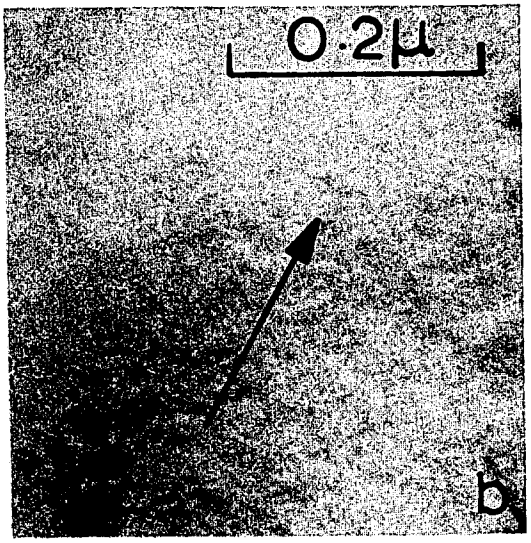


Fig. 3b



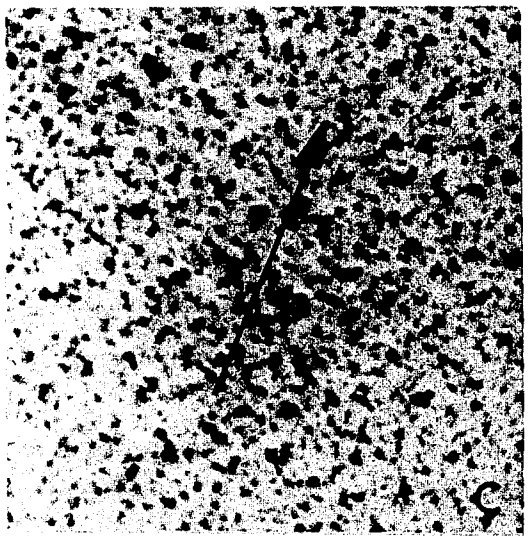


Fig. 3c

Fig. 5a

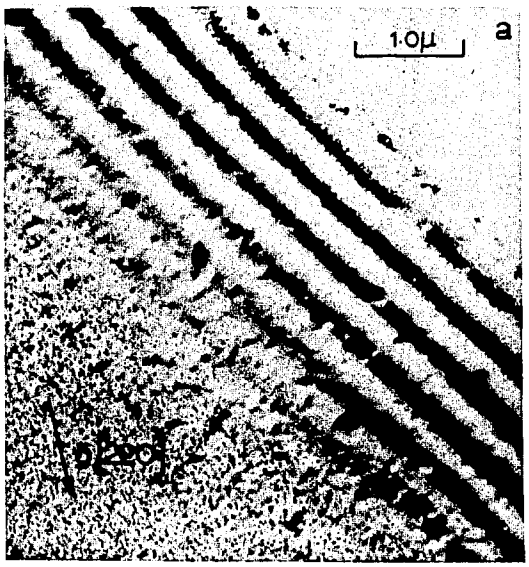
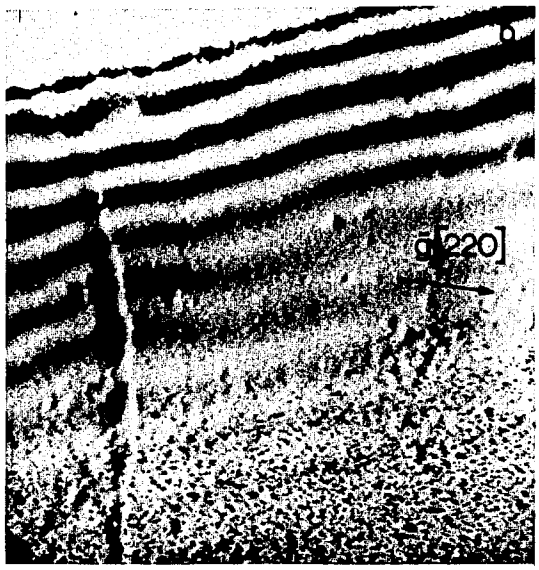


Fig. 5b



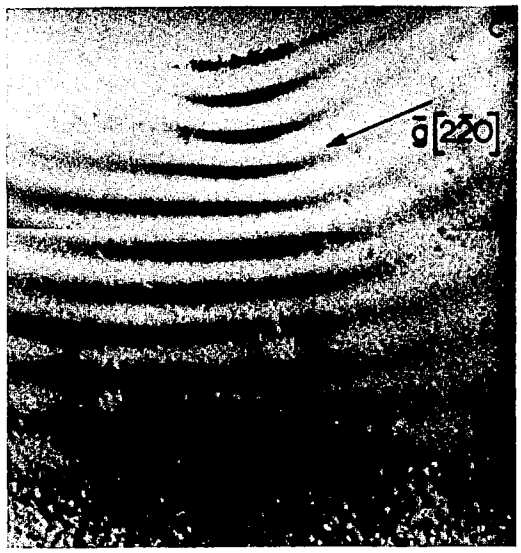
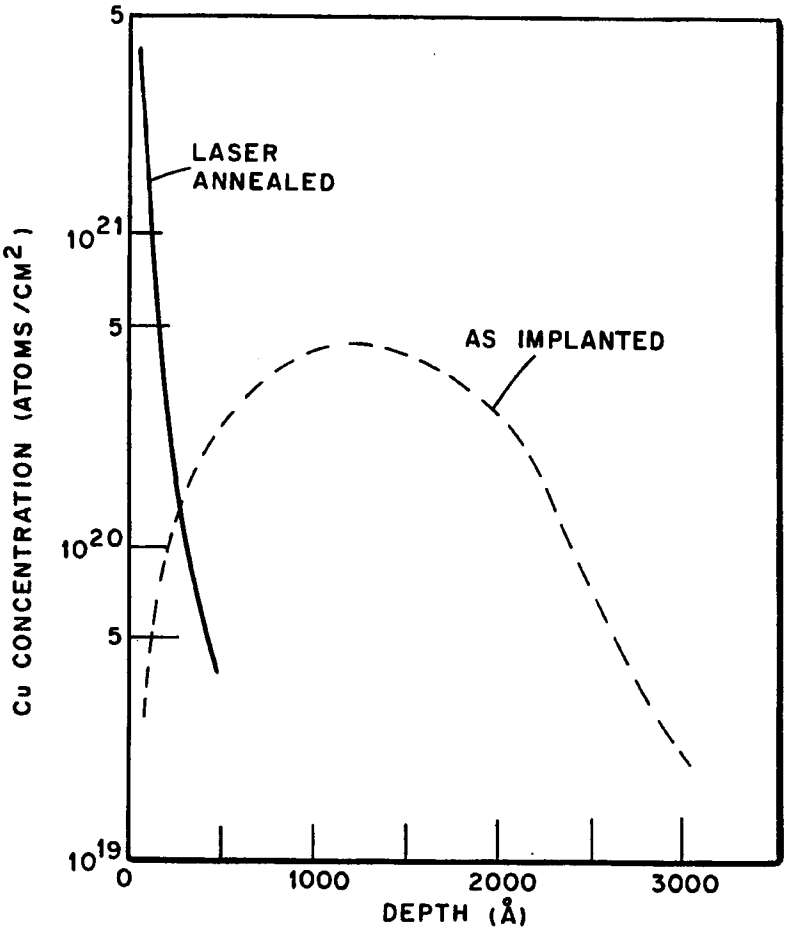


Fig 5c



$^{63}Cu^+$ (150 keV, $6.9 \times 10^{15}/cm^2$) in 111 Si

Fig. 6

Fig. 7

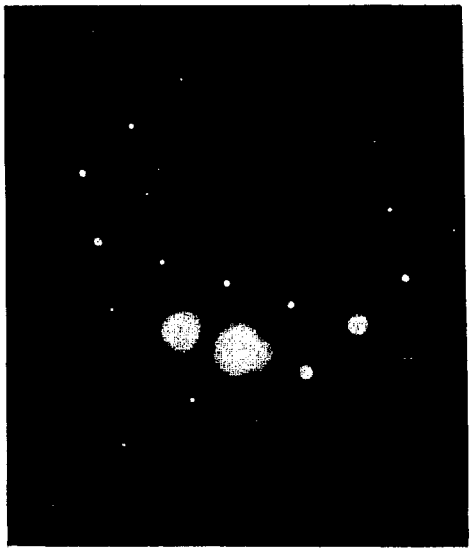


Fig. 8

METHOD FOR MAKING DEFECT-FREE ZONE BY LASER-ANNEALING OF DOPED SILICON

This invention was made in the course of, or under, a contract with the United States Department of Energy. The invention relates broadly to methods for annealing n-type and p-type silicon to improve its quality with respect to semiconductor applications. More particularly, the invention relates to the use of relatively high-power laser pulses to effect such improvement by localized melting.

As applied to n-type and p-type silicon bodies which have been doped with an impurity to form an electrical junction therein, the invention effects a significant improvement in the electrical parameters of the junction by eliminating doping-induced defects. For instance, the invention may be used to remove lattice defects generated by high-voltage ion implantation techniques. In another application, it may be used to electrically activate "dead layers" produced by conventional high-temperature-diffusion doping. In a third application, it may be used to remove electrically inactive precipitates and lattice defects from n-type and p-type silicon before it is doped to form an electrical junction therein. Again, it may be used for segregating impurities such as copper and iron in a near-surface region of a semiconductor material. The impurities so segregated then may be removed from the material.

BACKGROUND OF THE INVENTION

The most widely used process for the production of an electrical junction in silicon is high-temperature diffusion of boron into an n-type substrate or phosphorus into a p-type substrate. It is well known that such diffusion usually results in a "dead layer" of electrically inactive dopant precipitates. Thus, the diffused layer contains a region (the dead layer) which is characterized by an extremely short minority carrier lifetime. High-temperature diffusion of dopants also generates dislocations and dislocation loops in the diffused layer, and these imperfections adversely affect important electrical characteristics of the junction. Hitherto, there has been no effective method for annealing the diffused layer to electrically activate dopant atoms in the precipitates and remove dislocations and dislocation loops. The present invention meets this need.

Another conventional process for producing an electrical junction in an n-type or p-type silicon substrate is ion implantation, where the dopant is deposited by directing a high-density, high-energy beam of dopant ions into the substrate. Unfortunately, the energetic ions damage the crystal lattice, and most of the dopant ions are not electrically active because they are not in substitutional lattice positions. It has been the practice to thermally anneal the implanted layer to remove the damage and electrically activate the dopant, but such annealing does not completely remove the lattice damage. Furthermore, it leads to precipitation of dopants and contaminants in the implanted layer and to generation of impurity-related defects, all of which degrade various electrical properties, such as the minority-carrier lifetime. The present invention can be used to anneal ion-implantation layers much more effectively.

Various publications describe the laser treatment of n-type and p-type silicon. The following are examples of articles relating to the laser-annealing of ion-implanted silicon substrates: (1) E. I. Shtyrkov et al, "Local Laser Annealing of Implantation Doped Semiconductor Layers," *Sov. Phys. Semicond.*, Vol. 9, No. 10 (October 1975); (2) I. B. Khaibullin et al, "Utilization Coefficient of Implanted Impurities in Silicon Layers Subjected to Subsequent Laser Annealing," *Sov. Phys. Semicond.*, Vol. 11, No. 2 (February 1977); (3) G. A. Kachurin et al, "Diffusion of Impurities As a Result of Laser Annealing of Implanted Layers," *Sov. Phys. Semicond.*, Vol. 11, No. 3 (March 1977). The following are examples of United States patents which relate to the laser-treatment of silicon: U.S. Pat. No. 3,458,368, "Integrated Circuits and Fabrication Thereof," R. R. Haberecht, July 29, 1969; U.S. Pat. No. 3,940,289, C. L. Marquardt et al, "Flash Melting Method for Producing New Impurity Distribution in Solids," Feb. 24, 1976; U.S. Pat. No. 4,059,461, "Method for Improving Crystallinity of Semiconductor Films by Laser Beam Scanning and Products Thereof," J. C. Fan et al, Nov. 22, 1977.

So far as is known, hitherto there has been no laser-annealing technique which achieves virtually complete removal of doping-induced defects from silicon without at the same time degrading the electrical properties (e.g., the minority-carrier diffusion length) of the substrate. For instance, previous investigations of treating ion-implanted silicon with a laser failed to realize that the mechanism of melting can be used to achieve complete removal of defects without degrading electrical properties of the silicon.

OBJECTS OF THE INVENTION

It is an object of this invention to provide a method for laser-annealing diffused layers produced by the high-temperature diffusion of dopants into n-type or p-type silicon substrates.

It is another object to provide a method for laser-annealing n-type or p-type silicon containing grown-in defects, the annealing being effected with at least one laser pulse whose wavelength, energy density and duration comprise a novel and highly effective combination of silicon-melting parameters.

It is another object to provide a rapid method for segregating undesired impurities such as copper and iron in a near-surface region of silicon semiconductor material, thus facilitating subsequent removal of the impurities from the material.

SUMMARY OF THE INVENTION

One form of our invention may be summarized as follows: In a process wherein a surface of a crystalline silicon substrate is doped with a thermally diffused impurity to form an electrical junction therein, thereby generating doping-induced defects in a surface layer of said substrate, the improved method for removing said defects without degrading the minority-carrier diffusion length in said substrate, comprising:

irradiating said layer with at least one laser pulse selected from one of (a) Q-switched ruby laser-generated pulses having a wavelength of 0.694 μm, an energy density in the range of from about 1.5 to 3.0 J/cm^2, and a duration in the range of from about 20 to 50 nanoseconds and (b) Q-switched YAG laser-generated pulses having a wavelength of 1.06 μm, an energy density in the range of from about 5 to 7 J/cm^2, and a duration in the range of from about 80 to 120 nanoseconds to effect melting of said layer.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 comprises two electron micrographs. FIG. 1*a* is a view of an ion-implanted silicon specimen after laser-annealing in accordance with this invention, showing a complete annealing of defects. FIG. 1*b* is a view of a similar specimen which was not laser-annealed but rather thermally annealed at 900° C. for thirty minutes, showing a high density of residual damage in the form of dislocations and loops. The scale is shown, and arrows indicate the directions of diffraction vectors used.

FIG. 2 is a graph showing boron-distribution profiles for silicon wafers (a) as-implanted with boron, (b) after thermal annealing in conventional fashion, and (c) after laser annealing in accordance with this invention.

FIG. 3 is a series of bright-field transmission electron micrographs. FIG. 3*a* shows dopant precipitates in boron-diffused silicon; FIG. 3*b* shows the same region after laser annealing in accordance with this invention; and FIG. 3*c* shows the laser-annealed region after being heat-treated in conventional fashion.

FIG. 4 is a graph comparing the boron-distribution profiles for an as-diffused boron-doped specimen and the same specimen after annealing in accordance with the invention.

FIG. 5 is a series of bright-field transmission micrographs of a phosphorus-diffused silicon layer irradiated with superimposed laser pulses in accordance with this invention. FIGS. 5*a* and 5*b* show the specimen after treatment with one and three pulses, respectively (pulse energy density 1.6 J/cm^2). FIG. 5*c* shows the specimen after further laser treatment in accordance with the invention, as described in the text.

FIG. 6 is a graph presenting copper-concentration versus depth curves for a crystalline silicon body (a) after ion-implantation of copper and (b) after subsequent laser irradiation in accordance with this invention.

FIG. 7 is an electron-micrograph of a section of the above-mentioned ion-implanted, laser-irradiated specimen, and

FIG. 8 is a selected-area diffraction pattern for the same specimen.

DESCRIPTION OF THE PREFERRED EMBODIMENT

This method of annealing is applicable to the removal of various defects present in surface layers of n- or p-type silicon crystals. The crystal may or may not contain an electrical junction. As used herein, the term "defects" includes both lattice imperfections (e.g., dislocations and dislocation loops) and electrically inactive dopant precipitates. As applied to a body of semiconductor material, the term "surface layer" is used herein to mean a layer thereof which extends inward from a surface of the body for a distance of less than five microns. The term "removing defects" includes (1) the elimination of lattice imperfections and (2) the dissolution of precipitated dopant atoms into the silicon.

An important feature of our invention is to effect annealing by melting essentially all of the silicon layer containing doping-induced defects—e.g., radiation-bombardment-generated defects in the case of ion-implanted substrates. Another feature is that melting is accomplished with one or more laser pulses, each of which has a wavelength, energy density, and duration selected to melt the silicon effectively to the desired depth while avoiding degradation of electrical parameters in the substrate. For example, using a Q-switched ruby laser we employ laser pulses with a wavelength of 0.694 μm, an energy density of from about 1.5 to 3.0 J/cm^2, and a duration of from about 20 to 50 nanoseconds. We have found, for instance, that a laser pulse having a wavelength of 0.694 μm, an energy density of 1.6 J/cm^2, and a duration of 50 nanoseconds will melt an amorphous silicon substrate to a depth of 4000 A. If desired, the depth of melting can be increased by increasing the energy density of the laser pulse. Alternatively, a relatively small increase in the depth of the melting may be achieved by using multiple pulses or decreasing the pulse duration, while remaining within the above-specified ranges. In the typical application of this invention, the depth to which the doping-induced defects have extended is determined by any suitable technique, such as ion back-scattering. The pulse melting parameters then are selected accordingly to effect melting to substantially that depth. (In some applications, such as those relating to certain conventional deep-junction devices, melting beyond that depth may be desirable.) As an alternative to the Q-switched ruby laser, a Q-switched YAG laser may be employed (wavelength, 1.06 μm; pulse duration in the range of about 80–120 nanoseconds; energy density in the range of about 57 τ/cm^2). Given the teachings below, one versed in the art can determine by only routine experimentation which values within the aforementioned ranges are the optimum for effecting melting to the selected depth.

EXAMPLE 1

Laser-Annealed Ion-Implanted Silicon

The starting material for this experiment comprised conventional (100) single-crystal wafers of n-type silicon. The wafers (2×1 cm×1 mm thick) were sliced from an 80 Ω/cm, dislocation-free, floating-zone ingots. After degreasing and drying, the wafers were chemically polished in CP-6 solution (HF:CH_3COOH:HNO_3=1:1:2). The wafers then were rinsed in deionized water and dried. Following drying, the wafers were implanted with boron under conventional conditions. That is, they were implanted under high vacuum (2×10^{-8} torr) with 11_B+ (35 KeV, 1.5×10^{-6} amps cm^{-2}) in the range from 1×10^{14} to 9×10^{16} cm^{-2}. The wafers implanted at each dose were each split in half for comparative laser annealing and thermal annealing treatments. In accordance with this invention, part of the split samples were annealed with a single laser pulse to effect melting throughout the damaged layer—i.e., the region containing doping-induced defects. The damaged layer extended slightly beyond the dopant distribution. The laser annealing was conducted in air, using the Q-switched output of a conventional ruby laser (λ=0.694 μm; pulse duration, 30–50 nsec; energy density, 1.5–1.7 Joules/cm^2 per pulse). Thermal annealing was conducted in a quartz furnace, under a helium atmosphere. The samples were step annealed for thirty-minute periods at temperatures up to 1100° C.

Table 1 (below) compares the laser-annealed and thermally annealed samples in terms of carrier concentration (N_s), carrier mobility (μ), and sheet resistivity (ρ_s) in the implanted layer, as determined by van der Pauw measurements. The minority carrier diffusion length (L) in the annealed substrates was determined by surface-photovoltage measurements. In addition, the

utilization coefficient (ratio of N_s to the implanted dose D) is given. The table clearly shows that laser annealing under the conditions cited above provided better recovery of the electrical activity, with little or no degradation of the minority-carrier diffusion length. (As-received control samples—i.e., 80 Ω-cm material—had diffusion lengths in the range of 350-400 μm.) In marked contrast, thermal annealing at 900° and 1100° C. decreased the minority-carrier diffusion length significantly—i.e., by a factor of 5 or more. As shown, the carrier mobilities in the laser-annealed and the 1100° C. thermally annealed surface layers were in general agreement, allowing for a decrease of mobility with an increase in dopant concentration.

thermally annealed implanted specimens exhibited massive damage in the form of dislocation loops (average loop size, approximately 250 A), with a dislocation-loop density of approximately 1.0×10^{16} cm^{-3}, as shown in FIG. 1*b*. The complete removal of defects by the laser annealing is reflected in the comparative electrical measurements presented in Table 1.

The ion-implanted, laser-treated specimens subsequently were subjected to thermal annealing to study the clustering-point defects (single-vacancy or interstitial) and clusters thereof (if any) which might be below the microscope resolution (approximately 10 A). No clusters of defects were observed in the specimens which were implanted with doses not exceeding the

Table 1

Sample No.	Implanted Dose (cm^{-2}) D	Laser Annealing (Ruby Laser) λ = 0.694μ, E = 1.5-1.7 J/cm^2 = 30-50ns				Thermal Annealing									
						900° C./30 min.					1100° C./30 min.				
		N_s cm^{-2}	μ cm^2/v·s	ρ_s Ω/□	L μm	N_s cm^{-2}	μ cm^2/v·s	ρ_s Ω/□	L μm	N_s/D	N_s cm^{-2}	μ cm^2/v·s	ρ_s Ω/□	L μm	N_s/D
1	1.0×10^{14}	9.9×10^{13}	94	670	—										
2	4.2×10^{14}	5.0×10^{14}	54	230	340	3.2×10^{14}	64	307	80	.76	3.3×10^{14}	80	238	45	.79
3	1.0×10^{15}	1.5×10^{15}	41	102	295	6.5×10^{14}	53	179	70	.65	9.2×10^{14}	59	116	40	.92
4	5.0×10^{15}	7.5×10^{15}	35	24	275	1.3×10^{15}	42	114	70	.26	4.4×10^{15}	45	31	45	.88
5	1.0×10^{16}	1.5×10^{16}	31	13	350	1.6×10^{15}	39	103	75	.16	9.4×10^{15}	38	18	35	.94
6	2.5×10^{16}	3.8×10^{16}	30	4.3	—	4.2×10^{15}	30	51	70	.17	1.4×10^{16}	40	11	30	.56
7	6.0×10^{16}	Surface Cracking*				4.7×10^{15}	24	57	—	.08	1.5×10^{16}	39	11	—	.25
8	8.0×10^{16}	Surface Cracking*				4.7×10^{15}	23	58	—	.06	1.4×10^{16}	35	11	—	.18

*Observed after laser annealing

To compare the damage remaining in boron-implanted silicon samples subjected to laser and thermal annealing, studies were made using transmission electron microscopy (TEM) and 1 MeV He^+ ion backscattering. Samples for the TEM studies were prepared in the form of disks (3 mm diameter by 0.75 mm thick), using an ultrasonic cutter. These samples were dished from the back side in the center (1 mm diam.) to a depth of approximately 0.25 mm. Chemical polishing was used to remove any plastic damage. Nine such samples were implanted on the front side $11B+$ (35 KeV, 3×10^{15} ions cm^{-2}). Six of the samples then were laser-annealed under the above-specified conditions, and the remaining samples were thermally annealed at 900° C. for 30 min. The annealed samples then were chemically thinned from the dished side.

Electron micrographs of the annealed samples just described were taken under both bright- and dark-field (weak beam) imaging conditions for optimum visibility and contrast from defects. The thickness of the areas examined in the microscope varied from 0 to 5000 A (angstroms). In a typical instance the thickness of the area shown in the micrograph was 2000 A, which thickness included the peak-damage position (800 A) as well as the projected range of the ions (approximately 1150 A). As shown in FIG. 1*a*, *l no damage in the form of dislocations, stacking faults, and dislocation loops was observed. A* [100] electron-diffraction pattern showed no irregularity, confirming the perfection of the lattice of the implanted layer after laser annealing as described. (Similar results were obtained with unimplanted silicon wafers of the kind described above. That is, when unimplanted n-type wafers were laser-annealed under the same conditions as those employed with the boron-implanted wafers, micrographs showed removal of essentially all of the grown-in precipitates and lattice imperfections present in the unimplanted silicon.) In contrast to the laser-annealed implanted specimens, the equilibrium solid solubility limits. Electrical measurements of these specimens showed no change in carrier concentration.

In the specimens implanted with doses above the equilibrium solid solubility limit, thermal annealing of the laser-irradiated specimens led to precipitation of dopants. The decrease in carrier concentration could be correlated with the number of dopant atoms in the precipitates. These observations strongly suggest that there are no significant concentrations of defects (below the microscopic resolution) left after the laser treatment. One further advantage of laser annealing was that no dislocations were present near the junction due to the relaxation of strains produced by the implanted ions. This is in contrast to thermally annealed specimens, where the strain relaxation produces a network of dislocations near the junction, acting as recombination centers during operation of the device.

FIG. 2 shows the boron-distribution profiles for the samples discussed above. That is, profiles are shown for (a) as-implanted samples, (b) implanted and thermally annealed samples, and (c) implanted and laser-annealed samples. The data for FIG. 2 are based on secondary-ion mass spectrometry. As shown, the laser annealing effected pronounced changes in the implanted profile distribution. The nearly Gaussian as-implanted boron profile became almost uniform from the surface down to a depth of approximately 1800 A, and the profile broadened to a greater depth.

Using conventional techniques, solar cells were fabricated from silicon samples which had been laser-annealed in accordance with the invention. The cells were provided with three-layer Cr-Ti-Ag or Ti-Pd-Ag contacts. Silicon nitride or tantalum oxide (approximately 600 A thick) were used as anti-reflection coating materials. Table 2 presents important parameters for

these cells. The cell efficiency (14.5%, one-sun) is only slightly lower than those reported to date (approximately 16.1%) using the best conventional dopant-diffusion techniques and is much better (by a factor of 2) than that obtained by conventional thermal annealing of ion-implanted silicon. Further improvement in ion-implanted, laser-annealed solar cells can be expected by making shallower profiles and using back-surface fields.

Table 2

Cell No.	Junction Formation	Minority Carrier Lifetime in base material* $\tau(\mu s)$	Jsc(mA/cm^2)	AM 1 Parameters** Voc(mV)	FF	η(%)
IL 2	$^{11}B^+$ implant laser anneal (1.7 J/cm^2)	90	35	570	.72	14.5
IT 1	$^{11}B^+$ implant thermal anneal 900° C./30 min	5	13.7	465	.65	4.2+
IT 2	$^{11}B^+$ implant thermal anneal 1000° C./30 min	2.6	15.6	445	.61	4.4+
D 1	Boron diffusion 950° C./30 min	7	21.7	525	.66	7.5+

*Measured by surface photovoltage measurement.
**Tungsten lamp calibrated at approximately 100 mW/cm^2.
+ No antireflection coating (such a coating improves the efficiency by about 35%).

Still referring to Table 2, the improvement in open-circuit voltage V_{oc} is believed due to the more complete annealing of the implanted surface layer. The improved J_{sc} is believed due to the longer minority-carrier lifetime in the substrate and implanted layer. The data clearly show that the redistribution of dopants cannot be explained by thermal diffusion in the solid. The altered profiles were in good agreement with the theoretical calculations if it was assumed that the diffusion occurred in the liquid phase. The alteration in the profile was found to be dependent on both the pulse energy and the number of superimposed pulses. Measurements of quantum energy as a function of wavelength showed significant improvement in quantum response (electrons collected per incident photon) at all wavelengths. The improvement in the red region approached 70%; in the blue region it reached 25%.

In summary, although the ion-implanted samples were not optimized to provide maximum solar-cell performance, they exhibited one-sun conversion efficiencies much superior to those for the thermally annealed samples and comparable to those obtained with cells fabricated by standard high-temperature diffusion techniques. The increased activity of the laser-annealed samples correlated well with the great reduction in radiation-induced damage effected by laser annealing. In the past, ion implantation has not been favored as a technique in the production of solar cells because the subsequent thermal-annealing operation resulted in a very low-efficiency cell. With the present invention, ion implantation can be utilized to make solar cells of much higher efficiency.

Experiments similar to the above (laser-annealing and fabrication of solar cells) have been conducted with p-type silicon substrates implanted with one of the following dopants: phosphorus, arsenic, and antimony, in float-zone and Czochralski silicon (1–8 Ω-cm). These experiments also demonstrate that laser annealing to effect melting of the region containing radiation-induced defects resulted in junctions whose electrical parameters were significantly better than those of comparable samples which were thermally annealed.

EXAMPLE 2

Laser-Annealed Boron-Diffused Silicon Substrates

In this experiment the starting material comprised n-type (100) slices cut from a 5 Ω/cm phosphorus-doped, dislocation-free, float-zone silicon ingot. The wafers measured 2×1 cm×0.5 thick. After degreasing and rinsing, the wafers were chemically polished in CP-6 solution. Boron diffusions were carried out in conventional fashion—i.e., in an argon atmosphere with an induction furnace using a split graphite susceptor impregnated with B_2O_3. The diffusion conditions comprised 1100° C. for 10 min, 950° C. for 30 min, or 900° C. for 50 min. As will be described in Example 3, other wafers were diffusion-doped with phosphorus in conventional fashion, at 1100° C. for 60 min, using a PH_3 source.

In accordance with the invention, the resulting boron-doped silicon substrates were laser-annealed to effect melting throughout the diffused (boron-doped) layer to remove doping-induced defects therein—i.e., to eliminate dislocation loops and to dissolve and electrically activate dopant atoms in the dead layer (see above). The laser treatment was effected with the Q-switched output of a standard ruby laser (wavelength, 0.694 μm; energy density, 1.5–1.8 J/cm^2/pulse; pulse duration, approximately 50 nsec). The depth, or thickness, of the diffusion layer was determined by examining representative samples by means of stereoscopic electron-microscopy techniques. The typical diffused layer extended to a depth of 200 A.

The carrier concentration (N_s), carrier mobility (μ), and sheet resistivity (ρ_s) for the annealed wafers were determined by van der Pauw measurements. The dark-IV characteristics were measured on small mesa diodes (area, 1.115×10^{-3} cm^2), with an evaporated aluminum front contact and an electrolessly deposited nickel back contact. Transmission electron microscopy (TEM) studies were conducted with TEM-200 C and Hitachi 200 E electron microscopes.

Table 3 presents the results of van der Pauw measurements for the boron-diffused wafers before and after laser annealing. The results show clearly that the free-carrier concentration was increased considerably by the laser treatment. Moreover, the carrier concentrations near the surface on laser-treated samples D2 and D3 were 1.0×10^{21} and 1.5×10^{21} cm^{-3}, respectively, as determined by anodic oxidation and stripping techniques. These values are much higher than the solubility limit of boron in silicon. This increase in carrier concentration indicates that the electrically inactive precipi-

tates in the diffused samples were dissolved into substitutional sites by the laser annealing.

Table 3

Sample	Diffusion Temperature and Time	Before Laser Treatment N_s (cm^{-2})	ρ_s ($\Omega/\square$)	μ ($cm^2v \cdot s$)	After Laser Treatment N_s (cm^{-2})	ρ_s ($\Omega/\square$)	μ ($cm^2v \cdot s$)
D1	900° C./50 min	2.1×10^{15}	77	39	1.4×10^{16}	13.0	31
D2	950° C./30 min	3.8×10^{15}	44	38	2.5×10^{16}	8.6	29
D3	1000° C./10 min	5.8×10^{15}	28	38	3.4×10^{16}	6.3	30

The dissolution of the precipitates was confirmed by TEM studies. FIG. 3*a* is a micrograph illustrating the precipitates observed in Sample D2near the surface, in the as-diffused condition. The generally spherical precipitates exhibit black-white contrast characteristics which are expected from boron precipitates. The average size (third moment of the diameter) and the number density of the precipitates were determined to be 97.4 A and 3.2×10^{11} cm^{-2}, respectively. From stereomicroscopy it was found that the precipitates were contained in the first 200-A thick layer. As illustrated in FIG. 3*b*, laser treatment in accordance with this invention virtually eliminated doping-induced defects; that is, no precipitates or other defects (e.g., dislocation loops) were observed. The number of density of boron atoms contained in the precipitates was estimated to be $(1.85 \pm 0.25) \times 10^{16} cm^{-2}$. If it is assumed that all precipitates were dissolved during laser treatment and that the boron atoms were electrically activated, then the electrically active boron concentrations after laser annealing should have been $(2.23 \pm 0.25) \times 10^{16}$ cm^{-2}. The electrical measurements (Sample D2, Table 2) were in good agreement with this value.

Since the near-surface free-carrier concentration after laser annealing was much greater than the equilibrium solubility limit of boron in silicon, annealed Sample D2 was heated to 950° C. for 30 min to study the reprecipitation of boron. As indicated in FIG. 2*c*, the result was a distribution of generally spherical particles whose average size (third moment of the diameter) was determined to be 61 A. Black-white dynamic dark-field conditions indicated that the precipitates were centers of compression, as expected for boron precipitates. The amount of boron contained in these precipitates was 90% of that present in the as-diffused sample (FIG. 3*a*). Stereomicroscopy established that these precipitates were distributed almost uniformly up to 4500 A from the surface. These findings support the conclusion that the surface layer containing doping-induced defects was melted to about 4500 A by the laser pulse.

FIG. 4 is a boron-dopant profile of Sample D3 (Table 3), measured before and after laser annealing. As also observed by TEM, the high density of boron concentration is near the surface in the as-diffused sample, in the form of precipitates. As shown, the profile distribution was altered considerably by the laser treatment, the dead layer having been removed and the dopant redistributed farther into the crystal. This result, too, supports the conclusion that the surface layer containing the doping-induced defects was melted by the laser-annealing operation. Studies based on secondary ion mass spectrometry and ion backscattering showed that the alteration in boron distribution was dependent on the individual pulse energy and the number of superimposed pulses.

The influence of the laser annealing on the junction characteristics of the boron-diffused samples was examined before and after laser treatment. In both instances, the small mesa diodes followed closely the ideal diode equation

$$I = I_o[\exp \frac{qV}{AkT} - 1]$$

in the region of applied bias of 0.20 to 0.55 V. However, the diode perfection factor A in this region was improved from 1.5 ± 0.1 to 1.2 ± 0.1 by the laser annealing, indicating that recombination effects were decreased in the space-charge region.

Solar cells were fabricated from slices of boron-diffused Sample D2 (Table 3). The cells were provided with aluminum front contacts and electroless-nickel back contacts but were not provided with antireflection coatings, special texturized front surfaces, or drift-field back contacts. Laser annealing increased the J_{sc} parameter from an original value of 17.5 mA/cm^2 to 19.4. the V_{oc} parameter was increased from an original value of 520 mV to 540.

In summary, our method can be used to anneal diffusion-induced defects in the same manner as to anneal radiation-induced damage. That is, we anneal with one or more laser pulses, each having a wavelength, energy density and duration effecting melting throughout the surface layer containing doping-induced defects. More specifically, we anneal with pulses whose wavelength duration, and energy level are in the above-specified ranges for Q-switched ruby and YAG lasers. The depth of the layer containing doping-induced defects can be determined by any suitable technique, as by ion backscattering.

EXAMPLE 3

Laser-Annealed Phosphorus-Diffused Silicon Substrate

The starting material for this experiment was a p-type silicon wafer sliced from 15 Ω-cm (100) float-zone crystals. The resulting wafer was doped with phosphorus in conventional fashion—i.e., at 1100° C. for 60 min, with a PH_3 source. Precipitates (average size, 120 A; number density, 2.88×10^{15} cm^{-3}) and dislocation loops (average size, 200 A; number density, 0.92×10^{15} cm^{-3}) were observed. The precipitates exhibited strain contrast, analogous to compression centers. The dislocation loops were determined to be of the interstitial type. It was estimated from stereoscopic examination that the loops and precipitates were distributed inward from the surface to a depth of about one micron.

The phosphorus-diffused wafer was laser-annealed in accordance with this invention by irradiating the diffused layer with a series of laser pulses having a wavelength of 0.694 μm and a duration of 20 nanoseconds. As shown in FIG. 5*a*, one pulse of 1.6 J/cm^2 produced an annealed, defect-free region 0.55 μm deep. A second and similar pulse increased the depth of the defect-free region to 0.60 μm. After three such pulses the depth was determined to be 0.65 μm (FIG. 5*b*). Saturation in the depth of the annealed region was observed at 0.7

μm, after approximately five such pulses. The same region then was irradiated with a single pulse at an energy of 2.2 J/cm^2; this extended the annealed region to 0.9 μm (FIG. 5c). Complete annealing up to one micron was achieved by an additional laser pulse at 2.5 J/cm^2.

For phosphorus precipitates of average size 120 A, the time for dissolution by diffusion is estimated to be about 30 min (based on a diffusion coefficient of 10^{-10} cm^2/sec at 1325° C.); the corresponding time for boron precipitates is estimated to be about 60 min. For dislocation loops in phosphorus-diffused specimens, the time required for dissolution is about 10 min. Since the time that the laser-irradiated substrate is hot (≧1300°-1400° C.) is of the order of 200×10^{-9} sec, it is concluded that melting must be effected where diffusion coefficients are about 2.4×10^{-4} cm^2/sec.

It will be apparent to those versed in the art that our method as exemplified in Examples 2 and 3 is generally applicable to the annealing of diffused layers. That is, it is applicable to the annealing of n-type silicon into which an acceptor impurity has been diffused, and of p-type silicon into which a donor impurity has been diffused. Also, as mentioned in Example 1, it will be apparent that our method is applicable to the removal of the precipitates or lattice imperfections present in p-type or n-type silicon which has not been doped to form an electrical junction therein. That is, melting in accordance with this invention can be used to improve the electrical properties of crystalline silicon before it is doped by conventional junction-forming techniques, such as ion-implantation or high-temperature diffusion.

As mentioned, our method is based on our finding that doping-induced defects may be essentially completely removed by irradiation with laser pulses selected to effect melting at least to the depth of the silicon layer containing the defects. Our method may be conducted with any suitable laser, such as a ruby laser or YAG laser, operated in the Q-switched mode. The laser may be operated in the multi-mode or the uniphase mode. Better results were obtained with the uniphase mode because of Gaussian distribution of intensity across the beam.

The following example demonstrates the feasibility of using high-power laser pulses having a wavelength, duration, and energy level in the above-specified ranges to effect melting of a surface layer of a body of silicon semiconductor material in order to effect segregation of certain impurities in a near-surface region. The resulting impurity-rich layer then may be removed from the body by any suitable technique. The segregation technique is applicable, for instance, to the purification of n- or p-type silicon which is to be doped to form an electrical junction therein.

EXAMPLE 4

Single crystals of silicon (5 Ω-cm, n type, Cz) with (111) orientation were used in this experiment. Implants ($^{63}Cu^+$, energy 150 KeV, dose 6.9×10^{15} cm^{-2}) were performed at room temperature under high-vacuum conditions (2×10^{-8} torr). The resulting implanted specimens wre irradiated with single pulses of a Q-switched ruby laser ($\lambda=0.694$ μm; pulse duration, $\tau=50\times10^{-9}$ sec; pulse energy density, $E\approx1.6$ J cm^{-2}). Each specimen was divided for study by backscattering and electron microscopy techniques. Profiles of $^{63}Cu^+$ before and after the laser treatment were determined using 2.5 MeV He^+ ion backscattering in a high-depth resolution (30 A) scattering geometry. (The advantage of the high resolution case is increased sensitivity to detailed structure of the implanted impurity and to radiation damage profiles.) Channeling techniques were used to measure crystal perfection and to determine the lattice sites of dopant atoms. Specimens for transmission electron microscopy were prepared by a backthinning technique while protecting the implanted side.

FIG. 6 shows the concentration of copper as a function of depth before and after laser irradiation. The as-implanted specimen concentration profile has a Gaussian shape with the peak at about 1100 A. As shown, the laser treatment effects a significant change in the concentration profile, most of the copper now being segregated within 200 A of the surface. The channeling results also indicated that a significant recovery of crystal damage had occurred after laser irradiation because dechanneling in the <110> direction gave a "minimum yield" value of $x_{min}=5.7\%$ compared to $x_{min}=3\%$ for the virgin crystals.

Electron-microscope results showed that the displacement damage created by copper ions in the as-implanted samples had caused the implanted layer to become amorphous. After laser treatment, residual damage in the form of dislocation tangles and precipitates (P) was observed as shown in FIG. 7. Stereo microscopic measurements indicated that the residual damage was largely contained in the first 200 A with precipitates extending to about 400 A. Below this depth a defect-free crystalline region was observed. The residual damage, as observed by electron microscopy, was compatible with the high x_{min} values for these specimens. The dislocations were heavily decorated, presumably with copper silicide precipitates. Precipitates in the regions between the dislocations had average sizes (approx. 100 A) and exhibited black-white contrast under dynamical bright or dark field conditions. From the contrast behavior under both bright field and dark field conditions, these precipitates were tentatively identified as copper silicide (β-CuSi). Most of the copper was associated with precipitates near the dislocation tangles.

FIG. 8 is a selected area diffraction pattern showing that the implanted layer has crystallized in conjunction with the underlying (111) substrate. Similar results were obtained in the case of iron in silicon, where significant segregation of Fe to the surface was observed after the pulsed laser irradiation. For antimony in silicon, no precipitation was observed up to ion doses (^{121}Sb, 100 KeV) of 7×10^{15} cm^{-2}; however, precipitation of dislocations contained within about 400 A from the surface was observed for doses exceeding 1×10^{16} cm^{-2}.

As is known, Cu and Fe both have relatively low equilibrium distribution coefficients and solid solubility limits in silicon. Sb lies between (a) B, P and As (where no segregation is observed) and (b) Cu and Fe (where significant segregation is observed). Since a ruby laser pulse of $E\sim1.6$ J/cm^2 effects melting of silicon, it appears that the segregation of Cu and Fe near the surface may be the result of their low distribution coefficients and solubilities. In the process of solidifying molten silicon, the concentrations of Cu and Fe in the liquid far exceed those in the solid. Thus, we suggest that since the surface is the last region to solidify, segregation near the surface occurs. In many device applications involving silicon, Cu and Fe impurities act as very efficient recombination centers and adversely affect minority-carrier lifetime. Laser irradiation as described can be

used as a rapid purification treatment to segregate these impurities near the surface, where they can be removed by light etching of the surface or by any other suitable technique.

What is claimed is:

1. In a process wherein a surface of a crystalline silicon substrate is doped with a thermally diffused impurity to form an electrical junction therein, thereby generating doping-induced defects in a surface layer of said substrate, the improved method for removing said defects without degrading the minority-carrier diffusion length in said substrate, comprising:

irradiating said layer with at least one laser pulse selected from one of (a) Q-switched ruby laser-generated pulses having a wavelength of 0.694 μm, and energy density in the range of from about 1.5 to 3.0 J/cm^2, and a duration in the range of from about 20 to 50 nanoseconds and (b) Q-switched YAG laser-generated pulses having a wavelength of 1.06 μm, an energy density in the range of from about 5 to 7 J/cm^2, and a duration in the range of from about 80 to 120 nanoseconds to effect melting of said layer.

2. The process of claim 1 wherein said defects comprise precipitated dopant atoms.

3. The process of claim 1 wherein said substrate is n-type silicon and said impurity is a donor element.

4. The process of claim 1 wherein said substrate is p-type silicon and said impurity is an acceptor element.

5. In a process wherein an impurity is thermally diffused into a surface layer of a crystalline silicon substrate to form an electrical junction therein, the improved method for eliminating precipitates of said impurity in said layer without degrading the minority-carrier diffusion length in said layer, said method comprising:

determining the depth to which said precipitates extend in said layer, and

irradiating said layer with at least one laser pulse selected from one of (a) Q-switched ruby laser-generated pulses having a wavelength of 0.694 μm, an energy density in the range of from about 1.5 to 3.0 J/cm^2, and a duration in the range of from about 20 to 50 nanoseconds and (b) Q-switched YAG laser-generated pulses having a wavelength of 1.06 μm, an energy density in the range of from about 5 to 7 J/cm^2, and a duration in the range of from about 80 to 120 nanoseconds to effect melting of said layer to at least said depth.

6. The process of claim 5 wherein said substrate is p-type silicon and said impurity is an acceptor element.

7. The process of claim 5 wherein said substrate is n-type silicon and said impurity is a donor element.

8. A method for treating a surface layer of junction free silicon semiconductor material, said layer having dispersed therein an impurity selected from the group consisting of copper and iron to effect segregation of said impurity in a near-surface portion of said layer, said method comprising:

irradiating said layer with at least one laser pulse selected from one of (a) Q-switched ruby laser-generated pulses having a wavelength of 0.694 μm, an energy density in the range of from about 1.5 to 3.0 J/cm^2, and a duration in the range of from about 20 to 50 nanoseconds and (b) Q-switched YAG laser-generated pulses having a wavelength of 1.06 μm, an energy density in the range of from about 5 to 7 J/cm^2, and a duration in the range of from about 80 to 120 nanoseconds to effect melting of said layer.

9. The method of claim 8 further characterized by the step of removing from said layer the portion thereof containing the impurity so segregated.

* * * * *

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Francis et al. (43) Pub. Date: Mar. 27, 2003

(54) PROCESS TO CREATE BURIED HEAVY METAL AT SELECTED DEPTH

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(21) Appl. No.: 10/288,696

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(52) U.S. Cl. 257/566

(57) ABSTRACT

Semiconductor devices having recombination centers comprised of well-positioned heavy metals. At least one lattice defect region within the semiconductor device is first created using particle beam implantation. Use of particle beam implantation positions the lattice defect region(s) with high accuracy in the semiconductor device. A heavy metal implantation treatment of the device is applied. The lattice defects created by the particle beam implantation act as gettering sites for the heavy metal implantation. Thus, after the creation of lattice defects and heavy metal diffusion, the heavy metal atoms are concentrated in the well-positioned lattice defect region(s).

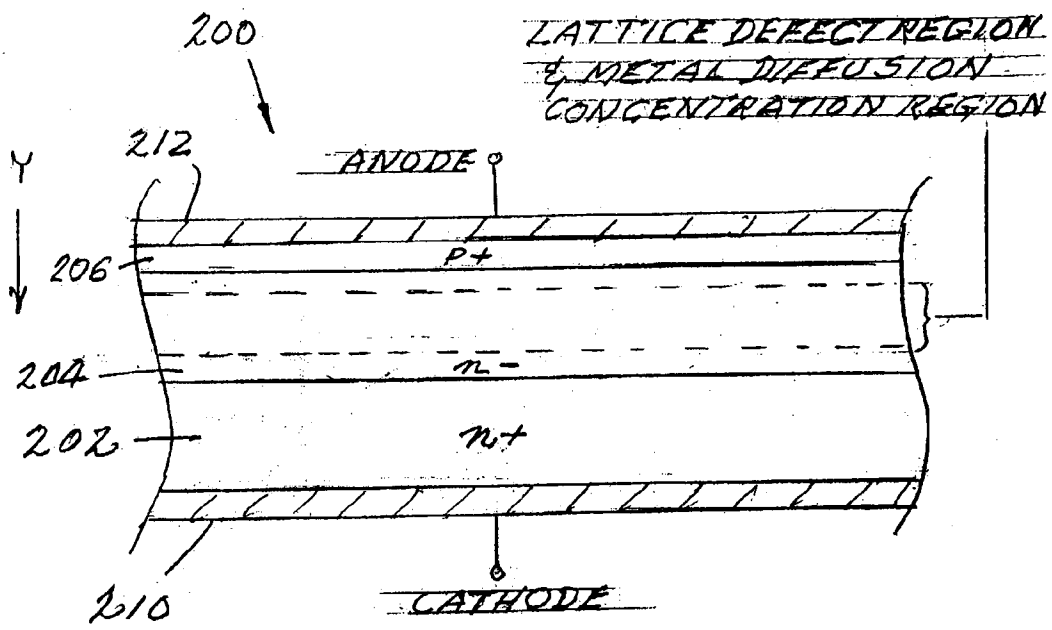
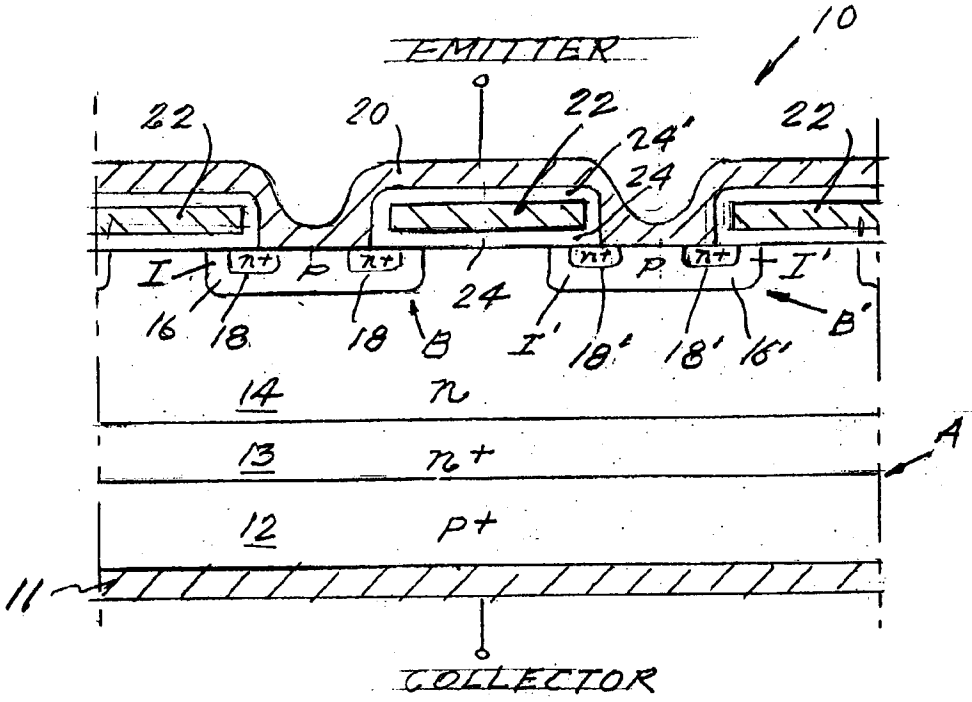


FIG. 1 PRIOR ART



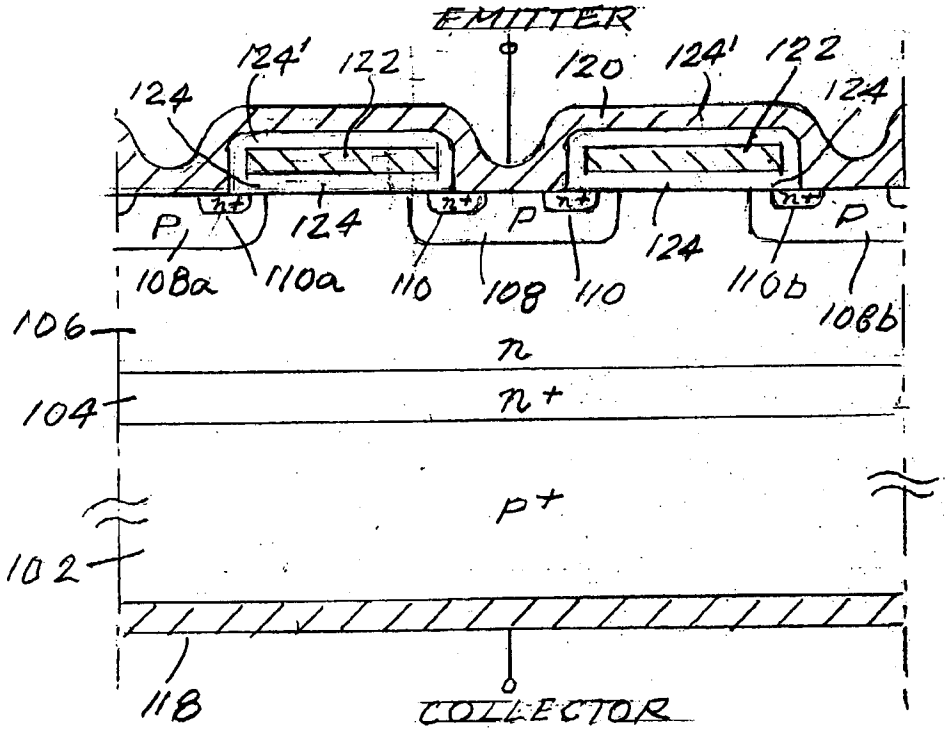
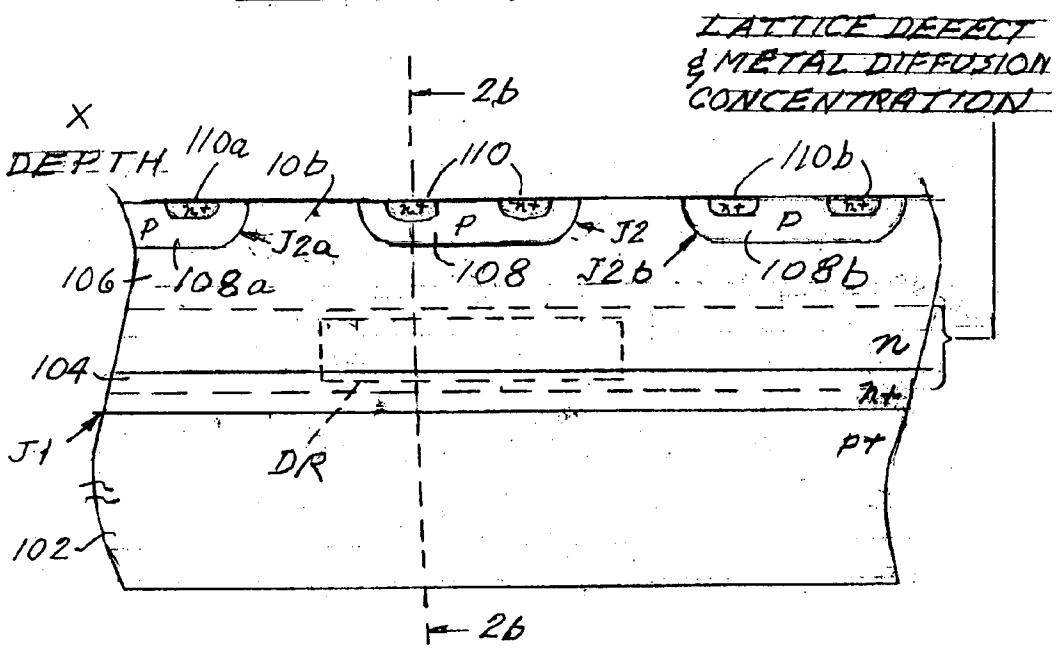


FIG. 2d

FIG. 2a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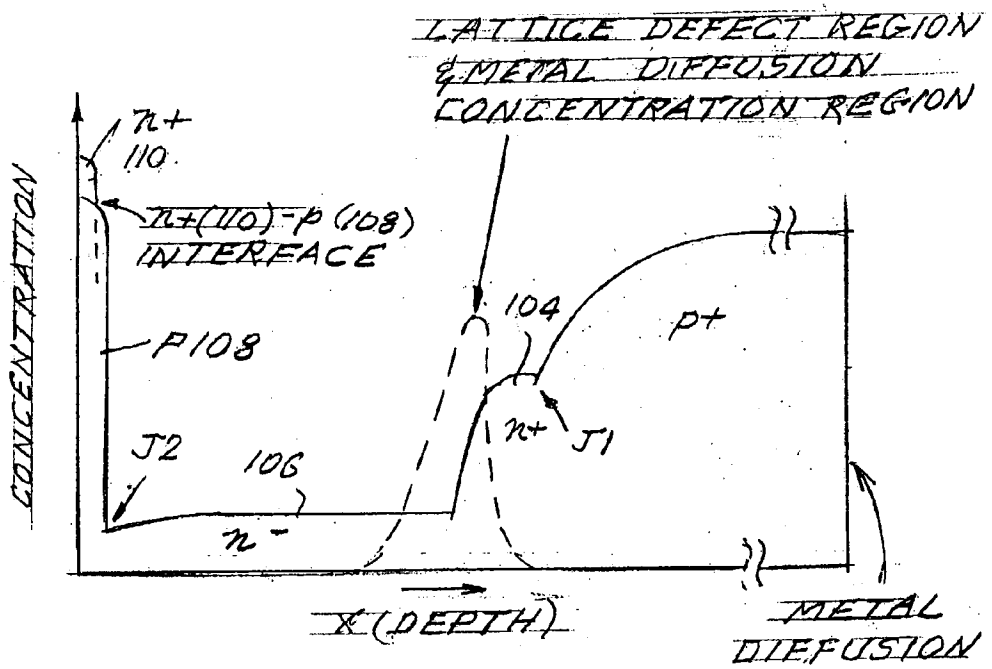
p+
102
2b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CONCENTRATION
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n+(110)-P (108) INTERFACE
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J2
106
n-
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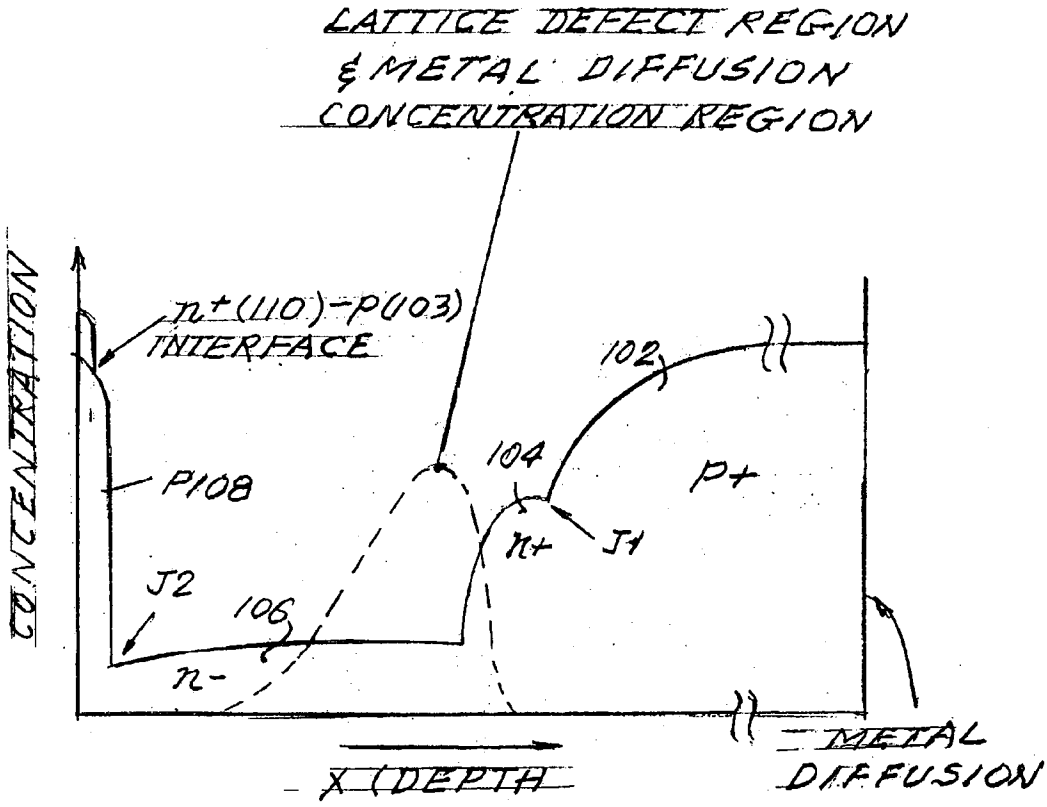
p+
n+
J1
X (DEPTH)
METAL DIFFUSION

FIG. 2b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& METAL DIFFUSION
CONCENTRATION REGION
CONCENTRATION
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INTERFACE
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P108
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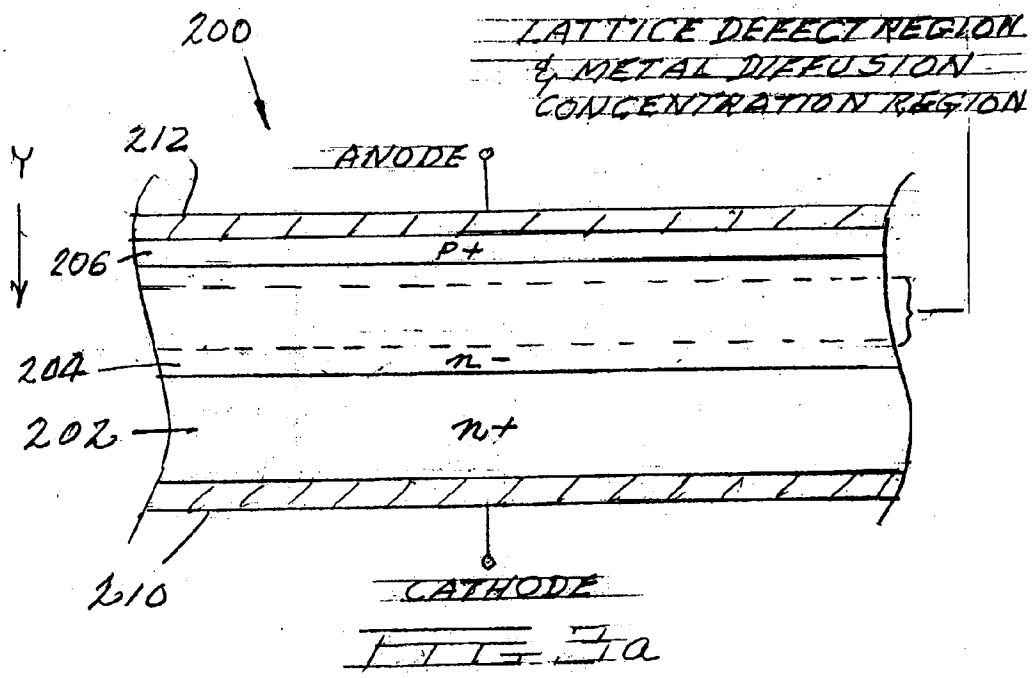
P+
n+
J1
J2
106
n-
METAL
DIFFUSION
X (DEPTH

FIG. 2c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& METAL DIFFUSION
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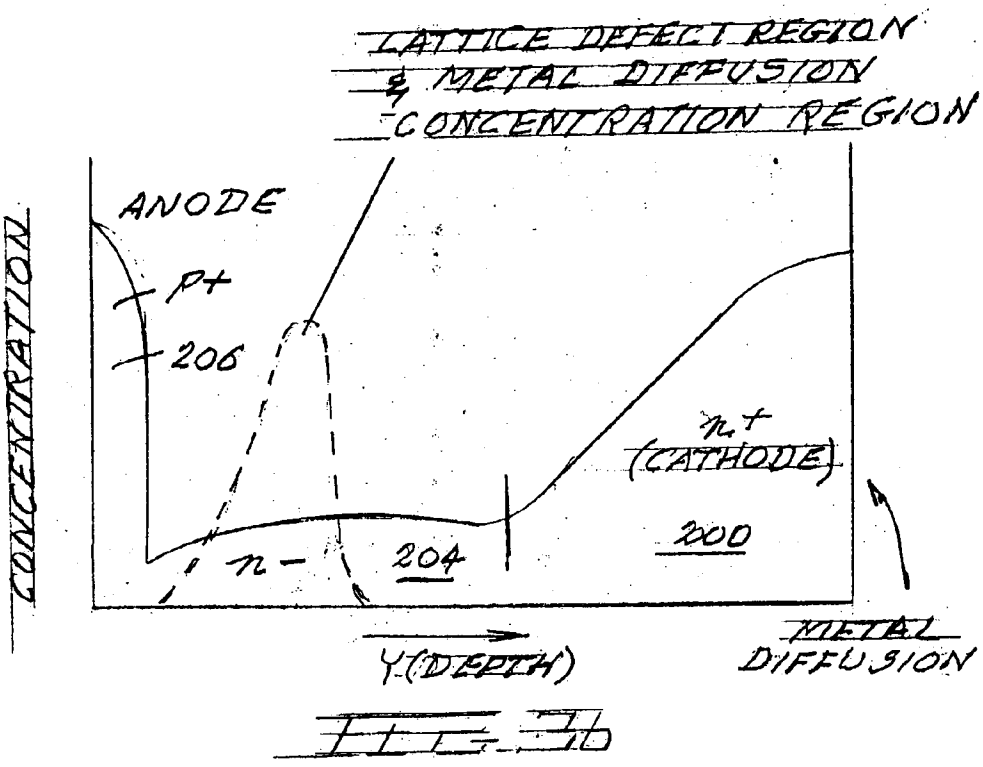
n+
210
CATHODE

FIG. 3a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& METAL DIFFUSION
CONCENTRATION REGION
CONCENTRATION
ANODE
P+
206
n+
(CATHODE)
200
n-
204
Y (DEPTH)
METAL
DIFFUSION

FIG. 3b

PROCESS TO CREATE BURIED HEAVY METAL AT SELECTED DEPTH

RELATED APPLICATION

[0001] This application is a continuation of U.S. application Ser. No. 09/593,472, filed Jun. 14, 2000 by Richard Francis and Chiu Ng entitled PROCESS TO CREATE BURIED HEAVY METAL AT SELECTED DEPTH

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The invention relates to power semiconductor devices, such as insulated gate bipolar transistors (IGBTs), diodes and thyristors. In particular, the invention relates to improving performance of such devices through reduction of lifetime (also known as "lifetime killing").

[0004] 2. Related Art

[0005] An IGBT **10** as generally known in the art is shown in **FIG. 1**. The IGBT **10** has collector electrode **11** connected to a p+ collector region **12**. Above collector region **12** is n+ type buffer layer **13** and n type base region **14**. A pn junction is formed at interface A between collector region **12** and n+buffer layer **13**. Typically, p+ collector region **12** is formed in the semiconductor wafer, while n+ buffer layer and n base region are epitaxially grown thereon. Base or channel diffusion regions **16**, **16'** of p material are formed at the upper surface of n region **14**, forming p bases, as explained further below. A pn junction is thus formed at the interfaces B, B'.

[0006] (As seen, there is an array of diffusion regions in the upper surface of n region **14**; one such adjacent region in the array is labeled with the same reference numbers including a prime designation. Additional analogous structure in the adjacent regions is also designated with a prime reference number.)

[0007] Within p-type diffusion region **16** is n+ diffusion region **18**. (There appear to be two separate n+ diffusion regions in the cross-sectional view of **FIG. 1**; however, the n+ diffusion region **18** is actually a closed loop within p diffusion region **16** when viewed from above when using a cellular base geometry as shown in U.S. Pat. No. 5,661,314, for example.) An emitter electrode layer **20** contacts the central portion of p diffusion region **16** and an interior portion of n+ diffusion region **18**.

[0008] A gate electrode **22** extends between the outer portion of n+ diffusion region **18** and the outer portion of n+ diffusion region **18'** of the adjacent diffusion region. Gate electrode **22** is interposed between the-surface of the semiconductor device **10** and the emitter layer **20** and is isolated from the surface of the semiconductor device **10** and the emitter electrode layer **20** by a conventional gate oxide **24** and a low temperature oxide (LTO) **24'**.

[0009] The IGBT of **FIG. 1** operates in a forward mode by applying a positive voltage at the collector electrode **11** with respect to the emitter electrode **20**. When gate **22** is biased to a voltage above the threshold voltage V_T, an inversion of p base region **16** occurs at the region I. A path is thus formed for electrons through emitter **20**, n+ diffusion region **18**, the inverted portion of p base region **16** and into n base region **14** and n+ buffer layer **13**. The pn junction A between this effective composite n region and the p+ region **12** is forward biased, thus providing a forward conducting state.

[0010] When the collector and the emitter are reversed biased, current flow is blocked because the pn junction at interface A is reversed biased.

[0011] An important operational parameter for many semiconductor devices, such as the IGBT described above, includes the switching speed or turn-off time. For example, when the device of **FIG. 1** is operating in its saturated on condition, there are a large number of minority carriers in the n+ and n-regions **13**, **14** and p+ region **12**. This concentration of holes and electrons, respectively, must be removed before the transistor **10** returns to its off condition.

[0012] There are a number of known techniques for reducing the lifetime of minority carriers in such semiconductor devices. Thus, additional recombination centers in one or more of the regions of the semiconductor device may be provided. An increase of the recombination centers may adversely affect other important operational parameters of the device, such as the forward voltage drop V_{ce}.

[0013] One such technique for reducing carrier lifetime is electron irradiation of the device. The irradiation creates lattice defects in the crystal, which act as recombination centers of minority carriers. Because there is a relatively high level of control over the energy, positioning and profile of an electron beam, the degree of damage to the lattice is relatively accurate. Damage created by electron irradiation can be uniformly distributed throughout the silicon, or can be limited to particular sites. A disadvantage of electron irradiation is that the damage to the lattice anneals out at relatively low temperatures, thus reducing the effectiveness of the lifetime killing. The degree of annealing can be affected by other factors related to manufacturing the device. Also, silicon devices subjected to this technique of electron beam (E-beam) radiation demonstrate higher reverse current leakage at elevated temperatures. Further, electron irradiation normally acts uniformly over the full lateral width of the device.

[0014] A similar technique of lifetime killing uses particle beam implantation. The lattice damage created by a particle beam is also highly accurate and controllable. The position and degree of the lattice defects are dependent on the size, mass and implant energy of the particle used, among other factors. Thus, the position of the lattice defects can be localized to a particular depth and profile in the silicon. Also, multiple recombination centers can be positioned at different locations throughout the device. However, like E-beam irradiation, damage created by low doses of particle beam implants also anneals out of the silicon at relatively low temperatures; also, devices implanted with particle beams have higher reverse current leakage at elevated temperatures.

[0015] Another and very common technique of lifetime killing introduces recombination centers into the silicon through diffusion of heavy metals, such as gold or platinum. Typical heavy metal diffusion temperatures are between 600 and 1000° C. The diffusion temperature controls the solid solubility of the metal atoms in the silicon and thus the density of the impurities. Consequently, lifetime decreases with higher diffusion temperatures. Because of the nature of the heavy metal recombination centers, in many cases the

devices have superior characteristics to those processed with electron irradiation or particle beam implants. Also, the recombination centers created by metal diffusion do not anneal out at the relatively low temperatures, as in electron irradiation or particle beam implants. However, heavy metal diffusion is a difficult process to control. Small variations in the processing conditions and/or the silicon used (for example, the substrate doping, manufacturing temperatures, etc.), can create a substantial variation in the lifetime killing, current amplification, forward voltage drop and other characteristics of the semiconductor device.

[0016] In general, techniques of fabrication of IGBTs such as that shown in **FIG. 1** are known in the art. Materials used in such fabrication are also known. Further, determining and administering electron irradiation or particle beam implantation to a particular semiconductor device in order to create recombination centers at particular regions which reduce lifetime but do not render other operational characteristics unacceptable is either known or can be determined through developed techniques. (For example, U.S. Pat. No. 5,661,314 describes fabrication of an IGBT having certain structural features for improving the packing density and increasing latch current. Use of electron irradiation, or, alternatively, heavy metal diffusion, for reducing lifetime is also described.) Also, determining and administering the appropriate conditions to improve the lifetime of a device by creating recombination centers through heavy metal diffusion (without rendering other operation parameters unacceptable) is also known or can be determined through developed techniques. As noted above, this includes appropriate placement of the regions of lattice defects or heavy metal diffusion to reduce lifetime while maintaining acceptable current amplification and forward voltage drop.

[0017] While both contribute to lifetime killing, as noted above the performance characteristics of recombination centers comprised of heavy metal diffusion and recombination centers created via electron irradiation or ion implantation are different. Thus, U.S. Pat. No. 5,747,872 teaches using both types of recombination centers in the same device in order to achieve soft switching and reduction of dynamic avalanche effects over a wider temperature range. The recombination centers provided by the heavy metal diffusion contribute to reduction of carrier lifetime that avoids the dynamic avalanche effect at lower temperatures, but causes large switching power losses (which contributes to dynamic avalanche effects) at higher temperatures. The recombination centers provided by the electron irradiation or ion implantation contribute to the performance at higher temperatures.

SUMMARY OF THE INVENTION

[0018] It is an objective to provide reduced lifetime in semiconductor devices while simultaneously minimizing the disadvantages found in the techniques of the prior art.

[0019] In particular, it is an objective of the present invention to provide regions of recombination centers in semiconductor devices that are accurately positioned and which are maintained under normal manufacturing and/or operating conditions of the device. The recombination centers reduce the lifetime of minority carriers at turn-off while other operational characteristics of the device, such as current amplification and forward voltage drop, are maintained at acceptable operating levels.

[0020] In accordance with these objectives, the present invention includes a method of generating recombination centers within a semiconductor device comprising the steps of creating at least one lattice defect region within the semiconductor device using particle beam implantation. Use of particle beam implantation positions the lattice defect region(s) with high accuracy in the semiconductor device.

[0021] Creating one or more lattice defect regions is followed by heavy metal implantation treatment of the device. The lattice defects created by the particle beam implantation act as preferential gettering sites for the heavy metal implantation. Thus, after heavy metal implantation treatment, the heavy metal atoms are concentrated in the lattice defect region(s).

[0022] The diffused heavy metal atoms create recombination centers that are positioned with the relatively high level of accuracy attendant to particle beam implantation. Thus, the precision of irradiation and implantation is combined with the stability and superior recombination aspects of heavy metal diffusion.

[0023] The combination provides a device which may be tailored so that the forward voltage drop and the switching speed (and switching loss) is optimized. As noted, additional recombination centers may generally increase the forward voltage drop of a device. On the other hand, by adding recombination centers, switching speeds are increased. (An increase in switching speed corresponds to a reduction in carrier lifetime. Also, switching loss, which arises from current fall time, is reduced with an increase in switching speed.) The invention provides a way to precisely tailor recombination centers comprised of heavy metal atoms using a select depth for the region, shape (including width) of the region and/or concentration (including a variable concentration) of the region. Introduction of the recombination centers thus increases the switching speed (and reduces the switching losses), while proper tailoring of the recombination centers reduces the adverse change in the forward voltage drop.

[0024] The invention also provides semiconductor devices with recombination centers comprised of heavy metals that are positioned in one or more well-defined regions of the device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] **FIG. 1** is a cross-sectional view of a known insulated gate bipolar transistor device;

[0026] **FIG. 2*a*** is a cross-sectional view of an insulated gate bipolar transistor device of the present invention without metal electrode and gate layers;

[0027] **FIG. 2*b*** is a graphic representation of the carrier concentration of the various regions of the semiconductor device of **FIG. 2*a***;

[0028] **FIG. 2*c*** is a graphic representation as in **FIG. 2*b***, showing an alternative configuration of the lattice defect region and heavy metal diffusion concentration region;

[0029] **FIG. 2*d*** is a cross-sectional view of the insulated gate bipolar transistor device of **FIG. 2*a*** with metal electrode layers;

[0030] **FIG. 3*a*** is a cross-sectional view of a diode which employs the present invention; and

[0031] **FIG. 3***b* is a graphic representation of the carrier concentration of the various regions of the diode of **FIG. 3***a*.

DETAILED DESCRIPTION

[0032] **FIG. 2***a* illustrates an insulated gate bipolar transistor device **100** according to the present invention. N+ type buffer layer **104** is epitaxially grown on the surface of p+ doped substrate **102**, and n-layer **106** is epitaxially grown on buffer layer **104**. Note, however, that the invention to be described can be used in connection with float zone, non-epi die, and to devices employing a transparent anode. P type diffusion region or base **108** is created at the surface of n-layer **106**. Typically, the device **100** will contain an array of such p type base diffusion layers with any desired topology. Two such adjacent diffusion regions **108***a*, **108***b* are seen in **FIG. 2***a*. While the ensuing discussion only refers to diffusion region **108** and related structure, there may be hundreds or even thousands of corresponding regions in the surface of the n-region, such as those shown in the adjacent diffusion regions having an "a" or "b" suffix.

[0033] (In **FIG. 2***a*, a basic IGBT is used to describe embodiments of the invention. There are many deviations from the underlying structure shown in **FIG. 2***a* which can improve certain operational parameters for certain conditions and applications. For example, U.S. Pat. No. 5,661,314 cited above has two components of the p region corresponding to p region **108** in **FIG. 1**, and also has an n+ region between p diffusion regions. The IGBT in **FIG. 2***a* has been depicted at a more fundamental level, in order to focus on the inventive features of the present invention.)

[0034] Within p diffusion region **108** there is a ring shaped n+ diffusion region **110**. As will be explained below in the description of **FIG. 2***d*, the finished device has gates and electrodes similar to the device shown in **FIG. 1**. Thus, diffusion region **110** forms the emitter layer, p diffusion region **108** (when inverted by a gate) forms the base along with n layers **104**, **106**, and p+ substrate forms the collector. The device has pn junctions as shown at positions **J1** and **J2**.

[0035] **FIG. 2***b* is a graphical depiction of the relative concentration of carriers in the regions of the IGBT of **FIG. 2***a* as a function of the depth X in the device. The solid graphical depiction represents the concentration along line **2***b*-**2***b* of **FIG. 2***a*, that is, through the emitter region **110** and the p base diffusion region **108**. As seen, n+ region **110** is a shallow, high concentration region, p base diffusion region **108** has a relatively high concentration, – layer **106** has a relatively low concentration, n+ region has an intermediate concentration and p+ region has a relatively high concentration.

[0036] The device of **FIGS. 2***a*, **2***b* is first subjected to particle beam implantation of appropriate type, energy, duration, shape, etc. to create lattice defects in the silicon at a certain region in the usual manner. One such irradiated region is shown in phantom in **FIG. 2***b* spanning n+ and – regions **104**, **106** of the base, where the most effective lifetime killing is desired in an IGBT. Thus, if the lattice defect region shown in **FIG. 2***b* is created by particle beam implantation, then the phantom portion of the graph shows the relative concentration of the particles so implanted. In the prior art, the device is then completed and packaged, and is subject to the alloying out of the particle beam damage.

[0037] As described above, the lattice defects themselves provide additional recombination centers. However, in accordance with the invention, the device is next subjected to a heavy metal diffusion using gold or platinum or the like, as represented in **FIG. 2***b*. The lattice defects caused by the beam irradiation or the like act as gettering sites for the metal atoms, so following the diffusion, metal atoms are also concentrated in the preferred region shown in phantom in **FIG. 2***b* and are not evenly diffused through the silicon lattice as in the prior art.

[0038] The lattice defect region is chosen so that it is remote from the pn junctions **J1** and **J2**. Thus, the impact of the recombination centers introduced by the metal diffusion on the current gain and forward voltage drop is lessened while lifetime (and switching loss) is reduced.

[0039] The lattice defect region need not extend laterally throughout the package at a certain depth, but instead may be shaped to customized contours through control of the particle beam implantation. For example, referring back to **FIG. 2***a*, an alternative lattice defect region DR shown in phantom is limited to an area below diffusion region **108**, instead of generally extending throughout the device normal to the X direction, as in the embodiment also shown in **FIG. 2***a* and described above. Thus, the switching of the current from diffusion region **108** would be faster than other diffusion regions. By creating lattice defect regions in a select manner, the performance of the device may be modified.

[0040] As noted, while additional recombination centers generally increase the switching speed (by reducing lifetime), they may also increase the forward voltage drop of a device. In general, the configuration of a lattice defect region (i.e., the depth, width, concentration of defects) and the resulting heavy metal recombination centers may be tailored so that the effect on the forward voltage drop is minimized while the switching speed of the device is nonetheless increased. Thus, an increase in the forward voltage drop from an increased dose of irradiation (which results in increased lattice defects and an increase in the number of heavy metal recombination centers gettered in the lattice defect region) can be offset by tailoring the configuration and position of the lattice defects and recombination centers.

[0041] **FIG. 2***c*, for example, shows an alternative configuration of the recombination center region shown graphically in **FIG. 2***b*. In **FIG. 2***c*, the maximum concentration of the recombination centers is shifted to the left, and the concentration is not symmetric.

[0042] Adjusting the configuration and position of the recombination centers may, on the other hand, curtail the benefit in the switching speed of the device; however, the recombination centers may be configured so that an optimum balance point between forward voltage drop and switching speed may be achieved.

[0043] In general, desired or optimal placement, profile, concentration, etc. of the lattice defect region and the resulting metal diffusion concentration region is also dependent on the structure of the semiconductor device, the conditions of manufacture of the device, and the materials of the device, among other things. The data and techniques of simple electron irradiation, particle beam implantation or heavy metal diffusion may be used in the present invention to determine where it is desirable to position the recombi-

nation centers in various semiconductor devices, as well as the profile and concentration of such recombination centers.

EXAMPLE 1

[0044] An IGBT rated for 1200V having structure as depicted in **FIG. 2***a* and having the relative concentrations shown in **FIG. 2***b* is constructed with the following widths:

[0045] p+ region (**102**) approx. 375 microns

[0046] n+ region (**104**) approx. 12 microns

[0047] – region (**106**) approx. 100 microns

[0048] p region (**108**) approx. 4-5 microns

[0049] n+ region (**110**) approx. 0.3 microns

[0050] The structure is subjected to a particle beam implant of helium or hydrogen atoms through the back surface of the wafer using known techniques, dosages and energy to attain an implant profile of the concentration and position shown in **FIG. 2***b*. The beam is applied homogeneously across the surface. The implant creates a lattice defect region across the device at the interface of – layer **106** and n+ layer **104** (i.e., peak concentration of the lattice defect region at a nominal depth of 100 microns).

[0051] The device is then subjected to metal diffusion, for example, gold, palladium or platinum, through the back wafer surface, or lower surface of p+ region **102** at an appropriate temperature, concentration and time to attain the desired drive in. The heavy metal atoms concentrate in the lattice defect region described above at a concentration determined by the diffusion parameters. The device as fabricated has reduced lifetime without an unacceptable increase in forward voltage drop.

[0052] In general, the lattice defect regions for semiconductor devices such as IGBTs may be created using particle beam implantation of He or H atoms at a dose of 1×10^{11} to 1×10^{17} atoms/cm^2 and energy determined by the depth of the desired defect region, materials involved, etc. The heavy metal diffusion may use platinum or gold atoms at a temperature of 600 to 1000° C. The drive in time and dosage is determined by the depth of the defect region, the materials and the desired concentration of the metal concentration region.

[0053] The lattice defects created by the particle beam implantation need not necessarily precede the diffusion. The heavy metal may first be diffused into a region. Lattice defects may then be created at desired location(s) using particle beam implantation, which act as gettering sites for the metals. Additional heating may be required so that the metal atoms concentrate in the defect region.

[0054] After creation of the metal diffusion region shown in **FIGS. 2***a* and **2***b*, the gate **122**, emitter **120** and collector **118** layers are then fabricated as shown in **FIG. 2***d* using known fabrication techniques. Gate **122** is isolated by insulating layers **124, 124'**. The basic gate operation of the IGBT is as described above with respect to **FIG. 1**. Of course, an IGBT having doped regions opposite those shown in **FIG. 1** (i.e., a p channel DMOS pattern can be formed in the top die surface) may be fabricated in accordance with the invention. For an n channel DMOS structure, gold may be used as the heavy metal.

[0055] Although the present invention is particularly suited for creation of accurately positioned heavy metal recombination centers in IGBTs, it is generally suited to semiconductor devices where such properties are desirable. Another such device is a high speed diode such as that shown in **FIG. 3***a*. The high speed diode **200** is comprised of relative thick n+ float zone region **202** having an epitaxially deposited – region **204**. A thin p+region **206** is diffused into region **204**. The diode as shown in **FIG. 3***a* includes the metal electrode layers, in particular cathode electrode **210** on n+ region and anode electrode **212** on p+ region.

[0056] **FIG. 3***b* illustrates the relative carrier concentration in the three regions of the diode **200** as a function of depth Y into the device. A lattice defect region is created within the silicon in a manner similar to that described above for the IGBT. That is, after fabricating layers **202, 204, 206**, but before fabricating the metal electrodes **210, 212**, the diode is subjected to particle beam implantation. One or more lattice defect regions are then created in precisely determined locations within the silicon, and having an appropriate profile that is predetermined by whether electron irradiation or particle beam implantation is used, energy of the electrons or particles, type of particles, profile the beam, time and dosage and the incident surface used, among other factors. As noted above, the positioning and contours of such lattice defect regions using particle beam implantation is relatively precise and is either known or determinable using known techniques for a specific semiconductor device.

[0057] One such lattice defect region is shown in phantom in **FIG. 3***b*. The region is positioned in the – region **204**, slightly less than half-way between p+ region **206** and n+ region **202**. So positioning the lattice defect region provides additional recombination centers in the – region **204**, sufficiently far from the junction with the p+ region, where additional recombination centers would adversely affect other operational characteristics of the diode.

[0058] Because the regions of the diode are uniform, the lattice defect region would typically extend throughout the diode normal to the Y direction, as shown in **FIG. 3***a*. However, the lattice defect regions could be localized to particular regions if the design required. More than one lattice defect region and variable defect concentration over the defect region is also possible, depending on device requirements.

[0059] The device is then subjected to a heavy metal diffusion, as represented in **FIG. 3***b* in dotted lines. The lattice defects again act as gettering sites for the metal atoms; following the diffusion metal atoms are also concentrated in the lattice defect region shown in phantom in **FIGS. 3***a* and **3***b*. Thus, the metal atoms are positioned in the well-defined area created by the particle beam implantation, and provide recombination centers having superior characteristics to those provided by lattice defects alone. As noted above for the IGBT, the configuration (such as depth, width, concentration, shape) of the lattice defect region and resulting heavy metal combination centers may be adjusted to offset increases in the forward voltage drop, while maintaining desired increases in switching speed. If necessary, a configuration may be chosen to achieve an optimum balance between the forward voltage drop and the switching speed of the device.

EXAMPLE 2

[0060] A fast recovery diode rated for 600V having structure as depicted in **FIG. 3*a*** and having the relative concentrations shown in **FIG. 3*b*** is constructed with the following widths:

[0061] n+ region (**202**) approx. 250 microns

[0062] – region (**204**) approx. 60 microns

[0063] p+ region (**206**) approx. 6 microns

[0064] Before fabrication of the anode electrode **212** and cathode electrode **210** shown in **FIG. 3*a***, the device is subjected to a particle beam implant of helium atoms with a dose of from 5×10^{13} atoms/cm^2 to 1×10^{15} atoms per cm^2 using known techniques and appropriate energy to attain an implant profile of the concentration and position shown in **FIG. 3*b***. The beam is applied homogeneously across the surface. This creates a lattice defect region across the device at a nominal depth Y (for the peak concentration of helium atoms) of 25 microns and a lateral width of about 15 microns.

[0065] The device is then subjected to metal diffusion. Platinum is diffused into lower n+ region at a temperature of 600 to 1000° C. for 10 to 30 minutes. The exact temperature, time, concentration is tailored to attain the desired drive in. The platinum concentrates in the lattice defect region described above at a concentration determined by the diffusion parameters.

[0066] The device as fabricated has reduced lifetime without an unacceptable increase in forward voltage drop.

EXAMPLE 3

[0067] A fast recovery diode rated for 2000V having structure as depicted in **FIGS. 3*a*** and **3*b*** is constructed as follows:

[0068] n+ region (**202**) approx. 250 microns

[0069] – region (**204**) approx. 200 microns

[0070] p+ region (**206**) approx. 6 microns

[0071] Before fabrication of the anode electrode **212** and cathode electrode **210** shown in **FIG. 3*a***, the device is subjected to a particle beam implant of helium atoms with a dosage of approximately 1×10^{12} to 1×10^{15} atoms/cm^2 using known techniques and appropriate energy to attain an implant profile having the desired concentration and position. The beam is applied homogeneously across the surface. This creates a lattice defect region across the device at a nominal depth Y (for the peak concentration of helium atoms).

[0072] The device is then subjected to metal diffusion. Platinum is diffused into lower n+ region at a temperature of 600 to 1000° C. for 10 to 30 minutes. Again, the exact temperature, time and concentration is tailored to attain the desired drive in. The platinum concentrates in the lattice defect region described above at a concentration determined by the diffusion parameters.

[0073] The device as fabricated has reduced lifetime without an unacceptable increase in forward voltage drop.

[0074] As noted above, the invention is not limited to a particular semiconductor device, such as the IGBT and fast recovery diode examples given above. In general, the invention pertains to any semiconductor device where additional recombination centers are desirable or necessary. The one or more lattice defect regions may be created through electron irradiation, particle beam implantation, or a combination thereof. The lattice defect regions may extend throughout the semiconductor device or may be customized to a particular region within the device. How to create and accurately position such lattice defect regions (which provide recombination centers themselves) for particular semiconductor devices having particular materials in order to reduce lifetime, while preserving other operational characteristics of the device at acceptable levels, is either known or can be readily determined through known techniques.

[0075] According to the invention, the well-positioned lattice defect regions act as gettering sites for heavy metal atoms diffused into the device. The greater the degree of lattice defect, the more gettering of metal atoms in the region. In general, the selection of metals, concentration, diffusion temperature and time of exposure, among other conditions, to obtain a desired level of heavy metal diffusion is either known for particular devices having particular material layers, or is readily determinable. Since the lattice defect sites attract and thus concentrate the heavy metal atoms, diffusion parameters must be adjusted to account for such concentration from prior art diffusion parameters, which by themselves resulted in broader regions of recombination centers. Necessary adjustment of diffusion parameters is within the ability of one skilled in the art.

[0076] For all such devices, the configuration (such as depth, width, concentration, shape) of the lattice defect region and resulting heavy metal combination centers may also be adjusted to offset increases in the forward voltage drop, while maintaining desired increases in switching speed. If necessary, a configuration may be chosen to achieve an optimum balance between the forward voltage drop and the switching speed of the device.

[0077] Accordingly, although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. Thus, the present invention is not limited by the specific disclosure herein.

What is claimed is:

1. A method of fabricating a semiconductor device comprising the steps of:

a) providing a semiconductor die, having a top surface and a bottom surface;

b) creating a gettering site comprising at least one region of lattice defects having a varying concentration in the body of said die at a predetermined depth below the top surface, said region of lattice defects having a thickness within which the concentration of the lattice defects is between a maximum concentration level and a minimum concentration level;

c) diffusing heavy metal atoms into the semiconductor die; and

d) applying heat for a predetermined time sufficient to drive the heavy metal atoms into the lattice defects to form a region of lattice defect and heavy metal diffu-

sion that has a concentration profile which ranges between a minimum level and a maximum level.

2. A method of fabricating a semiconductor device as in claim 1, wherein the step of creating at least one region of lattice defects comprises particle beam implantation.

3. A method of fabricating a semiconductor device as in claim 1, wherein the semiconductor device is an insulated gate bipolar transistor.

4. A method of fabricating a semiconductor device as in claim 3, wherein the step of creating at least one region of lattice defects comprises creating lattice defects in the base region of the insulated gate bipolar transistor.

5. A method of fabricating a semiconductor device as in claim 4, wherein the at least one region of lattice defects is created in an n-type base region of the insulated gate bipolar transistor.

6. A method of fabricating a semiconductor device as in claim 5, wherein the step of subjecting the device to a diffusion of heavy metal atoms comprises a diffusion of platinum atoms.

7. A method of fabricating a semiconductor device as in claim 4, wherein the at least one region of lattice defects is created in a p-type base region of the insulated gate bipolar transistor.

8. A method of fabricating a semiconductor device as in claim 7, wherein the step of subjecting the device to a diffusion of heavy metal atoms comprises a diffusion of gold atoms.

9. A method of fabricating a semiconductor device as in claim 1 wherein the step of creating at least one region of lattice defects in the device serves to create gettering sites for the diffused heavy metal atoms.

10. A method of fabricating a semiconductor device as in claim 9 wherein the step of subjecting the device to a diffusion of heavy metal atoms serves to create recombination centers comprised of heavy metal atoms localized in the at least one region of lattice defects.

11. A method of fabricating a semiconductor device as in claim 10 wherein the step of creating at least one region of lattice defects in the device is performed before the step of subjecting the device to a diffusion of heavy metal atoms.

12. A method of fabricating a semiconductor device as in claim 10 wherein the step of creating at least one region of lattice defects in the device is performed after the step of subjecting the device to a diffusion of heavy metal atoms.

13. A method of fabricating a semiconductor device as in claim 10 wherein the step of creating at least one region of lattice defects in the device is performed simultaneously with the step of subjecting the device to a diffusion of heavy metal atoms.

14. A method of fabricating a semiconductor device as in claim 1, wherein the step of subjecting the device to a diffusion of heavy metal atoms comprises a diffusion of atoms selected from the group consisting of platinum and gold.

15. A method of fabricating a semiconductor device as in claim 1, wherein the semiconductor device is a diode.

16. A method of fabricating a semiconductor device as in claim 14, wherein the at least one region of lattice defects is created in an n-type cathode region of the insulated gate bipolar transistor.

17. A method of fabricating a semiconductor device as in claim 16, wherein the step of subjecting the device to a diffusion of heavy metal atoms comprises a diffusion of platinum atoms.

18. A semiconductor device comprising a semiconductor die having a top surface, and at least one region of lattice defects, the region located at a predetermined depth below the top surface and having a concentration of defects that is between a maximum concentration level and a minimum concentration level, wherein heavy metal atoms are diffused into the at least one region of lattice defects to provide a combined region of lattice defects and heavy metal diffusion that has a concentration profile that varies between a maximum level and a minimum level within the thickness thereof.

19. A semiconductor device as in claim 18, wherein the semiconductor device is an insulated gate bipolar transistor having an n type epitaxially grown base region, wherein the at least one region of lattice defects resides at least in part in the n type base region.

20. A semiconductor device as in claim 19, wherein the heavy metal atoms are platinum.

21. A semiconductor device as in claim 18, wherein the semiconductor device is an insulated gate bipolar transistor having a p type epitaxially grown base region, the at least one region of lattice defects residing at least in part in the p type base region.

22. A semiconductor device as in claim 21, wherein the heavy metal atoms are gold.

23. A method of fabricating a semiconductor device having forward voltage drop and switching speed requirements comprising the steps of:

a) providing a semiconductor die;

b) creating a gettering site comprising at least one region of lattice defects of a predetermined concentration profile, the concentration profile representing the combination levels of lattice defects along the thickness of the gettering site in the body of the semiconductor die; and

c) creating at least one preferential region of heavy metal recombination center in the at least one region of lattice defects by diffusing heavy metal atoms into the die and applying heat for a predetermined length of time to drive the heavy metal atoms into the lattice defects;

the configuration of the at least one preferential region of heavy metal recombination centers providing a forward voltage drop and a switching speed within the requirements of the device.

24. A method as in claim 23 wherein the configuration of the at least one region of heavy metal recombination centers is a function of the depth of the region in the device, the shape of the region and the profile of the concentration of recombination centers in the region.

25. A method as in claim 23, wherein the configuration of the at least one region of heavy metal recombination centers is selected to minimize the forward voltage drop while maintaining the switching speed above a threshold level.

26. A method as in claim 23, wherein the configuration of the at least one region of heavy metal recombination centers is selected to adjust the forward voltage drop in relation to the switching speed.

* * * * *

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United States Patent [19]

Oostra et al.

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[54] **IMPLANTATION METHOD HAVING IMPROVED MATERIAL PURITY**

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[52] **U.S. Cl.** **437/20**; 437/30; 437/36; 437/944

[58] **Field of Search** 437/30, 36, 944, 20; 148/DIG. 100

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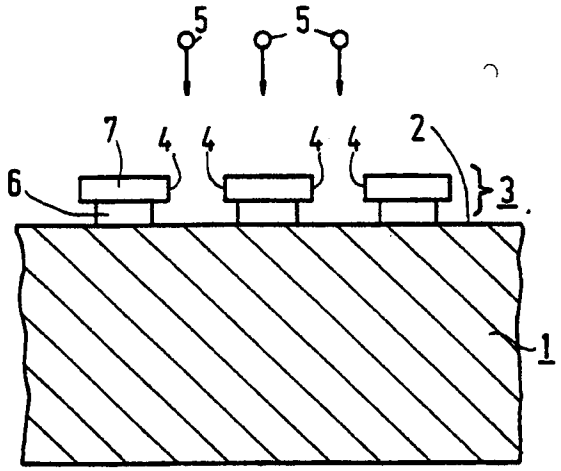
[57] **ABSTRACT**

A method of manufacturing a device, preferably a semiconductor device, whereby a mask (3) with an opening (4) extending down to a bare body (1) is provided on a surface (2) of this body (1), after which a substance (5) is implanted into the body (1) through the opening (4), upon which the mask (3) is removed. The mask (3) is provided by depositing a first and a second layer (6, 7, respectively) on the surface (2), and these layers are provided with the opening (4), while the first layer (6) can be selectively removed relative to the material of the body (1), and the second layer (7) is of the same material as the body (1). Since the same material is used for the second layer (7) as for the body (1), the body (1) is not polluted with material from the mask (3) in the opening (4) during implantation.

7 Claims, 3 Drawing Sheets



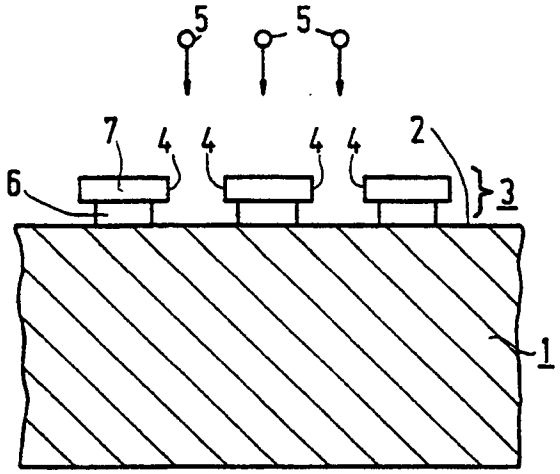


FIG.1

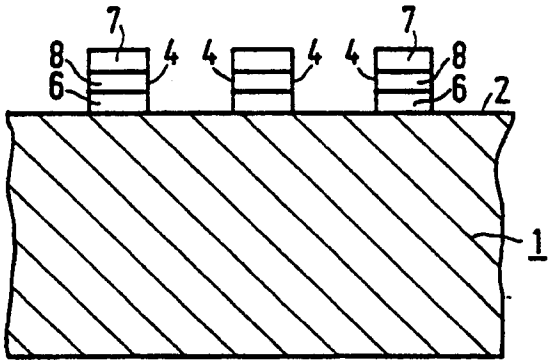


FIG.2

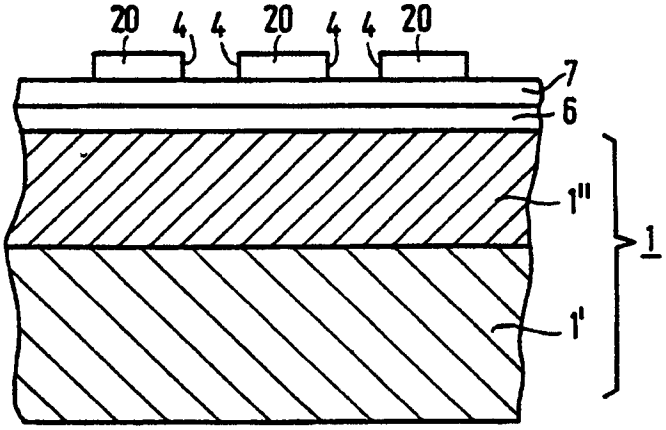


FIG.4

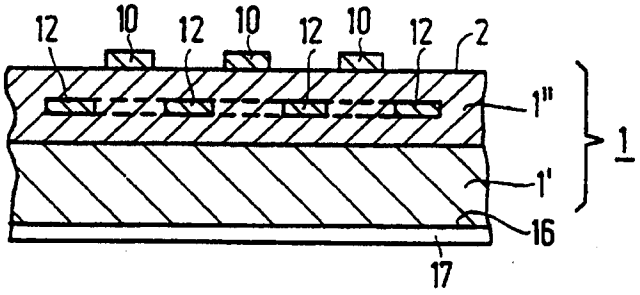


FIG. 3a

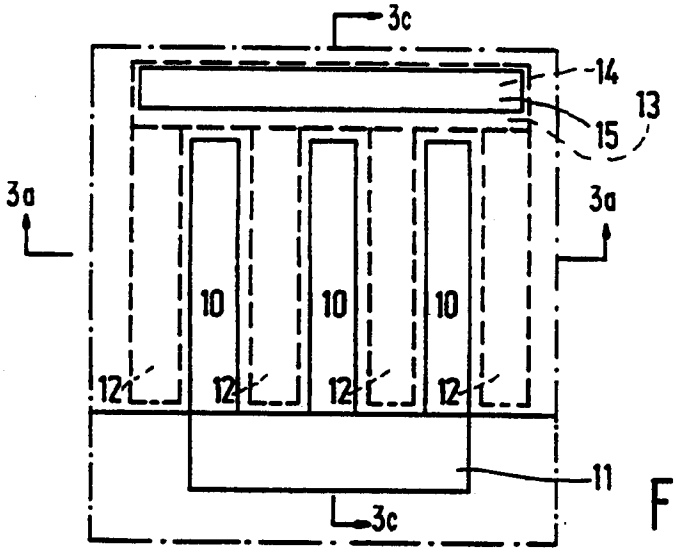


FIG. 3b

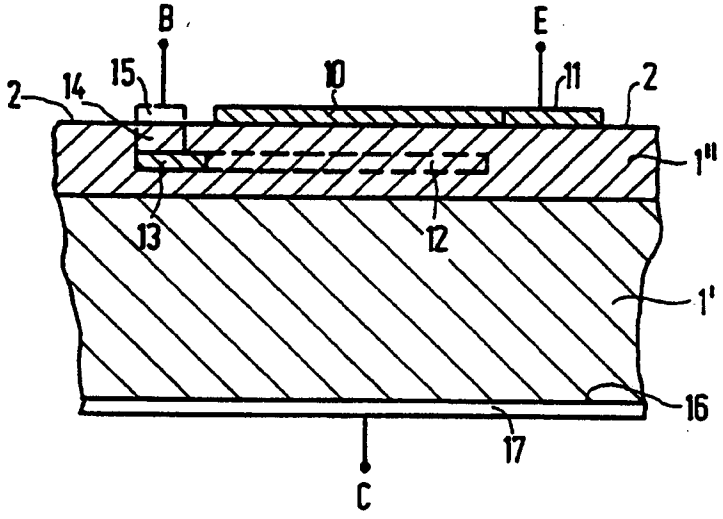


FIG. 3c

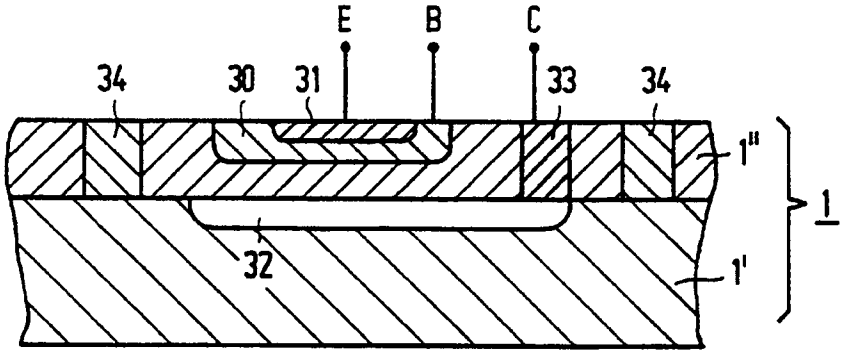


FIG.5

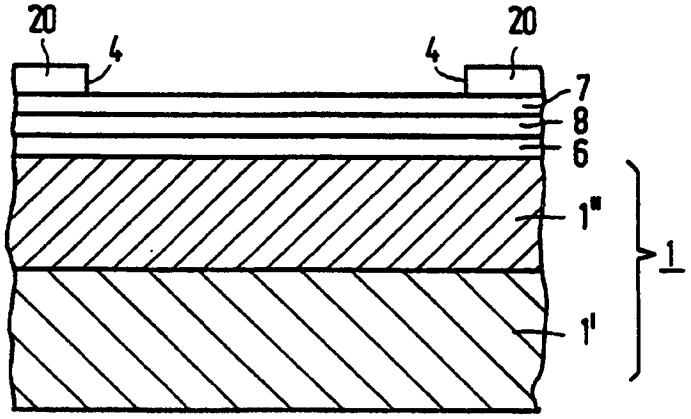


FIG.6

IMPLANTATION METHOD HAVING IMPROVED MATERIAL PURITY

BACKGROUND OF THE INVENTION

The invention relates to a method of manufacturing a device, preferably a semiconductor device, whereby a mask having an opening extending down to a bare body is provided on a surface of the body, after which a substance is implanted into the body through said opening, after which the mask is removed.

Such a method is particularly suitable for manufacturing semiconductor devices which, as transistors, are provided with buried conductor, semiconductor, or insulating layers. The substance then comprises, for example, Co, Ni, Ir, Fe, C, Y or O. Alternatively, for example, optoelectronic devices having optically active layers may be made by the method through the local implantation of ions of a rare earth metal into, for example, a glass body. The mask may comprise photoresist, silicon oxide, or, for example, a metal such as tungsten. The opening in the mask is made so as to reach down to the body, i.e. the body is bare in the opening, so that intermixing of any layer possibly present in the opening with the body during implantation is avoided.

A method of the kind mentioned in the opening paragraph is known from "Formation of Buried $CoSi_2$ by Ion Implantation" by K. Kohlhof et al. in Applied Surface Science 38 (1989), p. 207, whereby a silicon oxide mask is provided on a silicon semiconductor body. The opening is manufactured by lithographic techniques, whereby the silicon oxide is locally completely removed. A high dose of Co (approximately $3\ 10^{17}$ ions.cm^{-2}) is implanted into the semiconductor body at an energy of 200 keV through the opening. The mask screens the surface of the semiconductor body outside the opening against implantation by Co. The semiconductor body is kept at a temperature of 350° C. during implantation in order to repair part of the damage caused by the implantation. The implanted Co is convened into $CoSi_2$, which can function as a buried conductor layer, after heat treatments at approximately 700° C. and 1,000° C.

The known method described has the disadvantage that the semiconductor body below the opening is not only implanted with the substance Co, but that the semiconductor body is also polluted, so that electrical and chemical properties of the semiconductor body change. For example, when the silicon oxide of the mask is removed by etching, the semiconductor body is also affected by the etching in the opening.

SUMMARY OF THE INVENTION

The invention has for its object inter alia to counteract the said disadvantage.

According to the invention, the method is for this purpose characterized in that the mask is provided through consecutive deposition on the surface of a first and a second layer and by providing these layers with the opening, while the first layer can be removed selectively relative to the material of the body and the second layer comprises the same material as the body.

The invention is based on the recognition that pollution of the body during implantation takes place with material of the mask. Energetic ions of the substance collide with the mask material, whereby part of this material evaporates. Material of the mask is then included in the body through the openings. Evaporation of mask material takes place in all implantations, but especially when ions are implanted in a comparatively high dose, i.e. a dose higher than approximately 10^{16} ions/cm^2. During the manufacture of a buried conductor layer, for example, pollution of the body with mask material readily takes place. In the known method, silicon oxide of the mask is evaporated by the cobalt ions, whereby oxygen enters the semiconductor body through the opening. Owing to the inclusion of oxygen, the semiconductor body has become sensitive to an etchant for silicon oxide. When the mask is removed with an etchant for silicon oxide, the semiconductor body itself is then attacked as well. The use of the same material for the body and for the second layer, according to the invention, achieves that no pollution of the body takes place with mask material. In fact, the second layer is made of the same material as the body. So no foreign material enters the body. The mask is provided to such a thickness that the ions cannot reach the body through the mask.

It is noted that a method is known from the Japanese Patent Application JP 2-303 168 for forming a buried electrode in a silicon body by means of a polysilicon mask. An oxide layer is present over the entire surface of the body, so in the opening and between the mask and the body. The implantations take place through the oxide layer and the mask, so that mixing of oxygen with the body takes place in the opening and below the mask.

During the method, the substance is also implanted into the mask. In the known method, the substance can diffuse into the body situated below the mask during a further heat treatment, where it constitutes an undesirable impurity. In the method according to the invention, practically no diffusion of implanted substance from the mask to the body takes place because the first layer also acts as a diffusion barrier. The first layer also provides a good adhesion between the second layer and the body and at the same time ensures that the mask can be removed without damage to the surface of the body. This may take place, for example, in that the mask is covered with photoresist, the photoresist is etched back until only the openings are filled with photoresist, the second and first layer are removed by a usual etching technique, after which the photoresist is removed. Preferably, however, the mask is removed by a lift-off technique through the removal of the first layer, because this can be selectively removed relative to the material of the body. Thus the mask can be removed in a simple manner without attacking the body.

The first layer is removed during the lift-off. Portions of the second layer, however, may adhere to the body during the lift-off, since the second layer comprises the same material as the body. These remnants may be removed, for example, by polishing. Preferably, however, remnants of the mask are removed in a bath which is vibrated megasonically after the lift-off. A quicker and better removal of the mask is achieved in this manner.

When the openings in the first layer and in the second layer are equally large, the first layer may become locally exposed in the case of implantations of long duration or high energy owing to evaporation of an edge of the second layer near the openings, so that material of the first layer also evaporates and pollutes the body. Preferably, the method according to the invention is characterized in that the first layer is provided with a greater opening than the second layer. The second layer

will then completely overlap the first layer. No material of the first layer will become exposed near the opening when the edge of the second layer is evaporated, so that no pollution of the body with material of the first layer takes place. The opening in the first layer may be made greater than that in the second layer in a simple manner in that the first layer is underetched.

The mask is provided to such a thickness that the ions cannot reach the body through the mask. An average achievable penetration depth of the ions during implantation depends on the material into which they are implanted. In semiconductor materials, for example, a comparatively great penetration depth is possible. During implantation of such a body, according to the invention, the material of the second layer is also a semiconductor material, which means that a comparatively thick second layer must be provided to prevent ions entering the semiconductor body. Now it is difficult to provide openings with very fine details in comparatively thick layers. In such a case a first layer may be provided which can both be selectively removed relative to the body and has a small penetration depth for ions of the substance. Thus, for example, a comparatively heavy metal such as W may be taken for the first layer. Preferably, however, an intermediate layer of a material having a small penetration depth for ions of the substance is deposited after the deposition of the first layer, after which the second layer is deposited. The method then becomes more flexible. For example, a material may be taken for the first layer which forms a good diffusion barrier to the substance, but which does not necessarily have a small penetration depth for ions of the substance. A material is then deposited as an intermediate layer having a small penetration depth for the ions, so that a small layer thickness is required. The second layer again serves to counteract pollution caused by evaporation of mask material. The total thickness of the mask, especially in the case of implantations to a greater depth, may then be chosen to be smaller than would be the case without the intermediate layer, so that openings with very fine details can be provided in the mask.

When silicon is used as the material of the body, a glass, such as phosphorus silicate glass, or a metal, such as Ti or W may be used as the material for the first layer. An additional advantage is obtained when a first layer of silicon oxide or (oxy)nitride is deposited. A silicon oxide or (oxy)nitride layer may be deposited in a simple manner by usual techniques. In addition, etchants for silicon oxide and (oxy)nitride having a very good selectivity relative to silicon are available, while at the same time silicon oxide and (oxy)nitride can form a good diffusion barrier.

In the case of a silicon body, according to the invention, silicon is used as the material for the second layer. Preferably, a second layer of polycrystalline or amorphous silicon is deposited. Polycrystalline and morphus silicon can be provided in a very simple manner, for example, by deposition from the vapor phase (CVD).

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be explained in more detail below, by way of example, with reference to the drawing, in which:

FIG. 1 shows a mask comprising a first and a second layer, provided by a method according to the invention;

FIG. 2 shows a mask comprising an intermediate layer between the first and the second layer, provided by a method according to the invention;

FIGS. 3*a–c* show a so-called permeable base transistor with a buried base layer manufactured by a method according to the invention;

FIG. 4 shows a stage in the manufacture of a permeable base transistor;

FIG. 5 shows a power transistor comprising a buried conductor layer provided by a method according to the invention;

FIG. 6 shows a stage in the manufacture of a power transistor comprising a buried conductor layer.

The Figures are purely diagrammatic and not drawn to scale.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 shows a method of manufacturing a device, preferably a semiconductor device, whereby a mask 3 comprising an opening 4 extending down to a body 1 is provided on a surface 2 of the body 1, after which a substance 5 is implanted into the body 1 through the opening 4, upon which the mask 3 is removed again. During implantation, ions of the substance 5 are formed, which ions are so accelerated in an electric field that their energy (20 keV–4 MeV) is sufficient for them to penetrate through the openings 4 into the body 1. The ions of the substance 5 are neutralized in the body 1. The implanted substance 5 is incorporated in the body 1 by means of a heat treatment. Damage to the body created by the implantation is also repaired during the heat treatment. It is true especially for the formation of buried layers that, when comparatively large doses (for example, more than 10^{16} cm^{-2}) of a substance 5 are implanted, the damage to the body 1 is so great that a heat treatment after implantation is insufficient for repairing all damage. In such a case, the body 1 is kept at an elevated temperature of between approximately 300° C. and 500° C. during implantation. Part of the damage may then be repaired during the implantation itself. Buried or surface layers may also be structurally better owing to the implantation being carried out at an elevated temperature. The body 1 may comprise, for example, silicon, germanium or a glass, the mask 3 may comprise, for example, photoresist, silicon oxide, or a metal such as tungsten. The mask 3 may be provided in that a layer is deposited on the surface 2 of the body 1. The openings 4 are formed in this layer by photolithographic techniques and usual etching processes. After implantation, the mask 3 is removed from the surface 2 in that the material of the mask 3 is etched away selectively relative to the material of the body 1.

Implantation is frequently used, especially in semiconductor technology, for locally providing dopants or for manufacturing buried conductor layers or insulators. A problem arises in practice since the body 1 is polluted during implantation and properties of the body are adversely affected.

According to the invention, the mask 3 is provided in that a first layer 6 and a second layer 7 are consecutively deposited on the surface 2, which layers are provided with the opening 4, while the first layer 6 can be removed selectively relative to the material of the body 1 and the second layer 7 comprises the same material as the body 1. The invention is based on the recognition that material of the mask 3 evaporates through contact with energetic ions of the substance 5. The material of

the mask 3 evaporates especially when a comparatively high dose (for example, more than 10^{16} cm^{-2}) is implanted. The material of the mask 3 then pollutes the body 1 through the openings 4. Electrical properties such as conductance and chemical properties such as etchability of the body 1 may then change in an undesirable manner. In the method according to the invention, the layer with which the energetic ions come into contact is the second layer 7. This layer is made of the same material as the body 1. The material of the mask 3 which is evaporated by energetic ions of the substance 5 and which may possibly be incorporated in the body 1 is then the same material as that of the body 1 itself. Consequently, no pollution of the body with mask material takes place.

During implantation, the substance 5 is not only incorporated in the body 1 through the openings 4, but also in the mask 3. The mask 3 is provided to such a thickness that the ions cannot reach the surface 2 of the body 1 through the mask. During a heat treatment carried out during or after the implantation, however, the substance 5 is capable of diffusing from the mask 3 into the body 1. In the method according to the invention, the mask 3 is provided in that a first layer 6 and a second layer 7 are deposited. The first layer 6 acts as a diffusion barrier to the substance 5 implanted in the mask. The first layer 6, however, fulfils more functions. Thus this layer is also used inter alia as a bonding layer for the second layer 7, while the first layer 6 also serves to enable a selective removal of the mask 3 without attacking the surface 2 of the body. Materials which may be used for the first layer 6 are, for example, glasses or ceramic materials such as phosphorus silicate glass, oxides or nitrides, semiconductors such as silicon, or metals such as Ti or W. An exact choice of material for the first layer 6 may be made on the basis of known data about the degree of selectivity in etching of the first layer 6, about the degree to which the first layer 6 forms a diffusion barrier to the substance 5, and about the ease with which the first layer 6 is provided.

The mask 3 may be removed, for example, by covering the mask with photoresist, etching the photoresist back until only the openings 4 are filled with photoresist, and subsequently removing the second layer 7 and the first layer 6 by a usual etching technique, after which the photoresist is removed. Preferably, the mask 3 is removed by a lift-off technique through the removal of the first layer 6, since this layer can be selectively removed relative to the material of the body 1 according to the invention. The layer 6 may be removed in usual manner, for example, by a wet-chemical etching technique, whereby an etchant is used which selectively attacks the first layer 6, but does not affect the body 1. Thus the entire mask can be removed after use in a simple manner.

The first layer 6 is removed during the lift-off. Portions of the second layer 7, however, may adhere to the body 1 during the lift-off, after all this second layer 7 comprises the same material as the body 1. Preferably, remnants of the mask 3 are removed in a bath after the lift-off, the bath being vibrated megasonically. A quicker and better removal of the mask 3 is achieved in this manner.

The body 1 is implanted through the openings 4 in the first layer 6 and the second layer 7. Evaporation of the material of the second layer 7 may take place along an edge of the opening 4 in the case of long implantations. The material of the first layer 6 may then become exposed in such a location, after which material of the first layer 6 is also evaporated through contact with the ions of the substance 5. Since this material, in contrast to the material of the second layer 7, is different from the material of the body 1, this body 1 may become polluted. In the method according to the invention, the first layer 6 is provided with greater openings 4 than is the second layer 7, so that the second layer fully overlaps the first layer (see FIG. 1). No material of the first layer 6 will be exposed then when an edge of the second layer 7 near the openings 4 is evaporated, so that no pollution of the body 1 with material of the first layer 6 takes place. The openings 4 in the first layer 6 may be made greater than those in the second layer 7 in a simple manner through under-etching of the first layer 6, for example, with an isotropically etching wet-chemical etchant.

When ions are implanted into a body or layer of a certain material, these ions have a certain penetration depth which depends on, among other factors, their atomic weight, acceleration energy, and the material into which implantation takes place. Penetration depth is understood to mean the distance between the location in the body or layer where the concentration of the implanted substance shows a maximum and the surface of the body or layer through which the ions have penetrated the body. A concentration distribution of the implanted substance may then be characterized in usual manner by a spread σ. Many of the materials usual in semiconductor technology, such as silicon, silicon oxide, silicon (oxy)nitride, but also the usual photoresists have comparable penetration depths for ions. The mask 3 is provided to such a thickness that the ions cannot reach the body 1 through the mask 3. Since the material of the second layer 7 is the same material as the material of the body, a comparatively thick mask 3 will be required, especially when comparatively deep implantations are required. Now it is difficult to provide openings 4 with very fine details in comparatively thick layers. In such a case, a first layer 6 may be provided which can be selectively removed relative to the body and which also has a small penetration depth for the ions of the substance 5. For example, a layer of a metal such as molybdenum or tungsten, or of a different metal which is not too light, may be taken for the first layer 6. Preferably, however, an intermediate layer 8 of a material having a small penetration depth for ions of the substance 5 is deposited after the deposition of the first layer 6, upon which the second layer 7 is deposited and the openings 4 are provided (see FIG. 2). The method becomes more flexible then. A material may be taken for the first layer 6, for example, which forms a good diffusion barrier to the substance 5 and to the intermediate layer 8, but which does not necessarily have a small penetration depth for ions of the substance 5. A material having a small penetration depth for the ions is then deposited as the intermediate layer 8, so that a small layer thickness is required. The second layer 7 again serves to counteract impurities caused by evaporation of mask material. The total thickness of the mask 3 may then be chosen to be smaller than without the intermediate layer 8, so that openings 4 with very fine details can be provided in the mask 3.

When a body 1 made of silicon is implanted, an advantage is obtained when a first layer 6 of silicon oxide or (oxy)nitride is deposited. A silicon oxide or (oxy)nitride layer can be deposited in a simple manner by usual techniques. In addition, etchants for silicon oxide and

(oxy)nitride are available which show a very good selectivity relative to silicon, while at the same time silicon oxide and (oxy)nitride form a good diffusion barrier to many materials. According to the invention, silicon is then also used as the material for the second layer 7. Preferably, a second layer 7 of polycrystalline or amorphus silicon is deposited. Polycrystalline and amorphus silicon can be provided in a very simple manner by usual techniques, for example, through deposition from the vapor phase (CVD).

Embodiment 1: Implantation of a silicon semiconductor body with cobalt so as to form a buried layer for a "permeable base" transistor.

A permeable base transistor as outlined in FIG. 3 is manufactured by the method according to the invention. The Figure shows only one transistor for the sake of clarity, but in actual fact many transistors may be manufactured simultaneously in the semiconductor body 1. In FIG. 3, FIG. 3*a* is a cross-section taken on the line 3*a*—3*a* in FIG. 3*b*. FIG. 3*b* is a plan view of the transistor and FIG. 3*c* is a cross-section taken on the line 3*c*—3*c* in FIG. 3*b*. The permeable base transistor comprises a semiconductor body 1 built up from a highly doped n-type substrate 1' (10^{18} cm^{-3} As-doped) and a weakly doped n-type epitaxial layer 1'' (10^{15} cm^{-3} P-doped). The emitter is present at the surface 2 and is formed by a conducting layer in the form of fingers 10 which are interconnected by a metal layer 11. At a certain depth below the surface 2 there are buried conductor layers 12 in the form of fingers, forming a base electrode. The fingers 12 of the base electrode are connected to a buried conductor layer 13. This buried conductor layer 13 has an electrical connection to the surface through a highly doped n-type region 14. The highly doped region 14 is provided with a conductor layer 15 at the surface 2. A metal layer 17, which acts as the collector, is provided at a rear side 16 of the semiconductor body 1. The permeable base transistor is manufactured by the method according to the invention in that a first layer 6 of 50 nm thermal silicon oxide is grown through oxidation in wet oxygen (see FIG. 4) on the surface 2 of the silicon semiconductor body 1 in usual manner. A second layer 7 of 450 nm polycrystalline silicon is provided in usual manner on the first layer 6 by a low-pressure deposition from the gas phase (LPCVD). The polycrystalline silicon of the second layer 7 is subsequently provided with a photoresist 20 which is provided with openings 4 by photolithographic techniques and an etching process. The openings 4 are then provided in the second layer 7 in a plasma etching process comprising chlorine. Such an etching process etches polycrystalline silicon selectively relative to silicon oxide. Then the openings 4 in the first layer of silicon oxide 6 are etched in a reactive plasma etching process comprising carbon fluoride (CF_4) and hydrogen. This etching process is highly selective relative to silicon, so that only the first layer and not the semiconductor body 1 is attacked by the etchant. To make the openings 4 in the first layer 6 somewhat larger than the openings 4 in the second layer 7, the silicon oxide of the first layer 6 is lightly etched in an HF solution buffered with ammonium fluoride (1:7). The photoresist is then removed. FIG. 1 shows that the mask 3 provided with the openings 4 is then present at the surface 2 of the semiconductor body 1. Cobalt, i.e. the substance 5, is then implanted through the openings 4 at an energy of 400 keV up to a dose of 3.10^{17} cm^{-2} in order to form the buried conductor layers 12 and 13 for the base electrode. During the implantation the semiconductor body 1 is kept at a temperature of 450° C. so as to repair partly the damage caused during the implantation. Then the damage caused during implantation is repaired in two stages and the implanted cobalt is converted to highly-conductive buried layers 12 and 13 of cobalt silicide. During the first stage, the semiconductor body 1 receives a heat treatment for one hour at 600° C., a so-called "pre-anneal". During the second stage, a heat treatment at 1,000° C. for 30 minutes is carried out. After the second stage an approximately 100 nm thick cobalt silicide layer 12 and 13 has been formed at a depth of approximately 300 nm. Then the mask, which comprises the first layer 6 and the second layer 7, is removed through the removal of the first layer 6. To this end, the semiconductor body is introduced into a solution of HF (1:7) buffered with ammonium fluoride. The silicon oxide of the first layer is dissolved in this solution, so that the first layer 6 and the second layer 7 are removed from the surface 2. To remove any remaining mask portions, the semiconductor body is then megasonically vibrated in a solution of $H_2O_2/NH_3/H_2O$ (1:1:5). The surface 2 of the semiconductor body 1 is not attacked then. During the implantation no pollution of the semiconductor body 1 with material of the mask has taken place. Subsequently, the highly doped region 14 is formed in usual manner through, for example, a deep diffusion with P and the buried conductor layer 13 of the base electrode is connected to the surface 2. Then a metal layer, for example, cobalt is deposited on the surface 2 in usual manner, for example, by a sputtering process and this layer is patterned, whereby the emitter fingers 10 and the conducting layers 11 and 15 are formed. The rear side 16 of the semiconductor body is then provided with a metal layer 17, for example, an aluminum layer. The permeable base transistor thus created can be manufactured without short-circuiting between emitter and base taking place owing to etching attacks on the surface. The transistor manufactured has very good high-frequency characteristics.

Embodiment 2: Implantation of a silicon semiconductor body with nickel so as to manufacture a buried layer for a bipolar power transistor.

A cross-section of a bipolar power transistor is diagrammatically shown in FIG. 5. The Fig. shows only one transistor for the sake of clarity, but in actual fact many transistors may be manufactured simultaneously in the semiconductor body. The power transistor of the NPN type comprises a semiconductor body 1 constructed from a p-type doped substrate 1' and a weakly doped epitaxial n-type doped layer 1'' with a thickness of 11 μm. The p-type doped region 30 and the highly doped n-type region 31 are present in the epitaxial layer. The regions 30 and 31 act as the base and emitter regions of the transistor, respectively. At some depth below the surface 2 there is a buried conductor layer 32 which provides a low-ohmic connection to the collector. The conductor layer 32 has an electrical connection to the surface 2 through a highly doped n-type region 33. The highly doped p-type regions 34 serve to insulate the transistor. The power transistor is manufactured by the method according to the invention. To this end, a 50 nm thick first layer 6 of silicon nitride is deposited on the surface 2 of the semiconductor body 1 (see FIG. 6) by means of low-pressure chemical vapor deposition (LPCVD). A 0.5 μm thick tungsten intermediate layer 8 is deposited on the first layer 6 by a usual CVD pro-

cess from a mixture of WF_6 and H_2. A second layer 7 of 200 nm polycrystalline silicon is provided on this intermediate layer 8 in usual manner by low-pressure deposition from the gas phase (LPCVD). The polycrystalline silicon of the second layer 7 is then provided with a photoresist 20 which is given an opening 4 by photolithographic techniques and an etching process. The opening 4 is then provided in the second layer 7 in a plasma etching process comprising chlorine. The opening 4 in the tungsten intermediate layer 8 may be etched by means of a usual etching process with CF_4. Then the opening 4 is etched in the silicon nitride first layer 6 in a reactive plasma etching process comprising CH_2F_2. Nickel is then implanted as the substance 5 through the opening 4 at an energy of 2 MeV in a dose of 3.10^{17} cm^{-2} in order to form the buried conductor layer 32 for the collector connection. The semiconductor body 1 is kept at a temperature of 400° C. during the implantation in order to partly repair the damage done during the implantation. Then the damage caused during the implantation is repaired in two stages and the implanted nickel is converted to the highly-conductive buried layer 32 of nickel silicide. In the first stage, the semiconductor body 1 receives a heat treatment for one hour at 600° C., a so-called pre-anneal. In the second stage, a heat treatment at 1.000° C. is carried out for 30 minutes. After the second stage, an approximately 150 nm thick nickel silicide layer 32 has been formed at a depth of approximately 1 μm. Then the mask comprising the first layer 6, the intermediate layer 8 and the second layer 7 is removed through the removal of the first layer 6. To this end, the body is introduced into a solution of H_3PO_4. The silicon nitride of the first layer 6 is dissolved in this solution, whereby the first layer 6 as well as the intermediate layer 8 and the second layer 7 are removed from the surface 2 by a lift-off process. Remnants of the mask are eliminated in that the body is megasonically vibrated in a bath containing $H_2O_2/NH_3/H_2O$ (1:1:5). During implantation, no pollution of the body 1 with material of the mask has taken place. Subsequently, the regions 30, 31, 33 and 34 are manufactured in usual manner through diffusion of n- and p-type dopants. The emitter, base and collector regions are contacted by means of usual metal layers (not shown). The power transistor thus manufactured has very good characteristics. Thus the internal resistance of the collector is low and the transistor is capable of switching high powers.

Embodiment 3: Implantation of a silica glass body with erbium for the manufacture of a fluorescent layer for an optical device.

A 750 nm thick first layer 6 of silicon nitride is provided on a surface 2 of a body 1 of silica glass (amorphus silicon oxide) by means of an LPCVD process (see FIG. 1). A second layer 7 of 1.0 μm silicon oxide is provided on the first layer 6 through deposition from a tetraethoxy silane vapor (TEOS). The silicon oxide of the second layer 7 is subsequently provided with a photoresist which is given openings 4 by means of photolithographic techniques and an etching process. The second layer is provided with the openings 4 in a reactive plasma etching process comprising carbon fluoride (CF_4) and hydrogen. Then the openings 4 are etched into the first layer 6 of silicon nitride in a plasma etching process comprising CH_2F_2. This etching process is selective relative to silica, so that the first layer only and not the body 1 is etched. The photoresist is then removed. Subsequently, erbium is implanted as the substance 5 through the openings 4 at an energy of 3.5 MeV (Er^{++} ions) in a dose of 5×10^{15} cm^{-2}. The body 1 is kept at room temperature during the implantation. The damage caused during implantation is repaired in a standard furnace at a pressure of 10^{-6} Torr and a temperature of 900° C. during one hour. The implanted erbium is then present in a layer of approximately 0,5 μm thickness and a depth of approximately 1.25 μm below the surface 2. Then the mask comprising the first layer 6 and the second layer 7 is removed through the removal of the first layer 6. The body is introduced into a solution of H_3PO_4 for this purpose. The silicon nitride of the first layer 6 is dissolved in this solution, whereby both the first layer 6 and the second layer 7 are removed from the surface 2. No pollution of the body 1 with mask material has occurred during the implantation. The erbium layer exhibits strong fluorescence properties at a wavelength of 1.54 μm. Such a layer may be used in the construction of, for example, lasers and waveguides in optoelectronic technology.

It is noted that the substance may aim be implanted into a layer on a substrate. Thus, in the third embodiment, erbium may alternatively be implanted into, for example, a 10 μm thick silica glass layer on a silicon substrate. It is obvious that in such a case the expression "material of the body" should be read as "material of the layer".

The invention is not limited to the embodiments described above. The method according to the invention may be used whenever a very low pollution level the semiconductor body by the mask is desired during an implantation of a body.

We claim:

1. A method of manufacturing a device, in which a mask having an opening extending down to a bare body is provided on a surface of the body, after which a substance is implanted into the body through said opening, after which the mask is removed, characterized in that the mask is provided through consecutive deposition on the surface of a first and a second layer and by providing these layers with the opening, the first layer being selectively removable relative to the material of the body and the second layer comprising the same material as the body.

2. A method as claimed in claim 1, characterized in that the mask is removed by a lift-off technique by the removal of the first layer.

3. A method as claimed in claim 2, characterized in that remnants of the mask are removed in a megasonically vibrated bath after the lift-off.

4. A method as claimed in claim 1 characterized in that the first layer is provided with a greater opening than the second layer.

5. A method as claimed in claim 1 characterized in that an intermediate layer of a material having a small penetration depth for ions of the substance is deposited in the first layer, after which the second layer is deposited on the intermediate layer.

6. A method as claimed in claim 1, wherein the body comprises silicon, characterized in that the first layer comprises one of silicon oxide and (oxy)nitride.

7. A method as claimed in claim 6, characterized in that the second layer comprises one of polycrystalline and amorphus silicon.

* * * * *

US005236572A

United States Patent [19]

Lam et al.

[11] Patent Number: 5,236,572

[45] Date of Patent: Aug. 17, 1993

[54] **PROCESS FOR CONTINUOUSLY ELECTROFORMING PARTS SUCH AS INKJET ORIFICE PLATES FOR INKJET PRINTERS**

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[73] Assignee: **Hewlett-Packard Company**, Palo Alto, Calif.

[21] Appl. No.: **626,808**

[22] Filed: **Dec. 13, 1990**

[51] **Int. Cl.**[5] **C25D 1/08**

[52] **U.S. Cl.** **205/75**

[58] **Field of Search** 205/75

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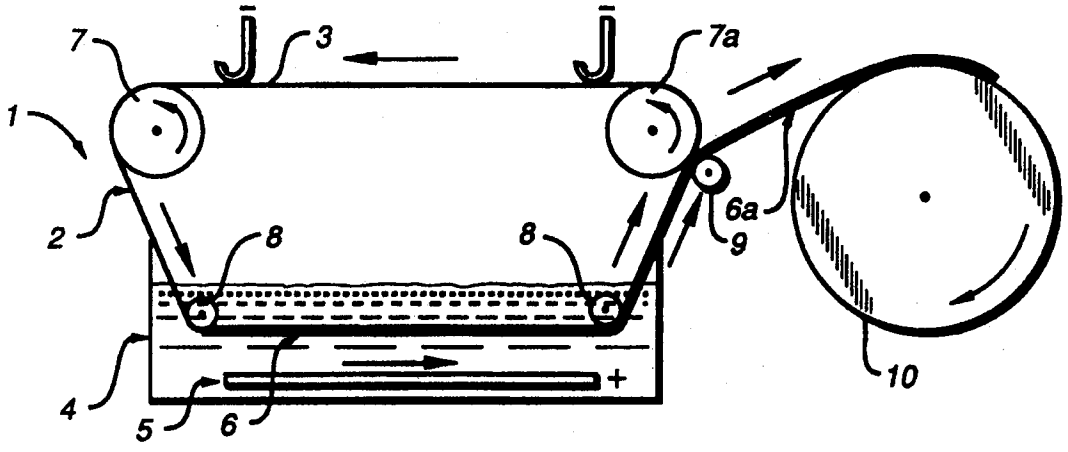
Primary Examiner—T. M. Tufariello

[57] **ABSTRACT**

A method for continuously manufacturing parts requiring precision micro-fabrication. According to the method, a surface of a mandrel having a reusable pattern thereon is moved through an electroforming bath. While the mandrel surface moves through the bath, a metal layer is deposited on the mandrel surface to define a pattern. After the metal layer has been deposited to the selected thickness, the metal layer is separated from the mandrel surface.

16 Claims, 1 Drawing Sheet



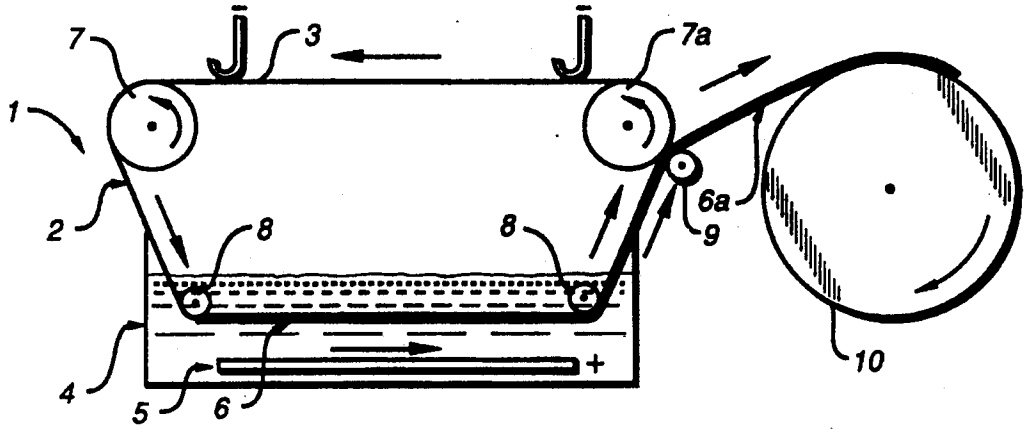


FIG._1

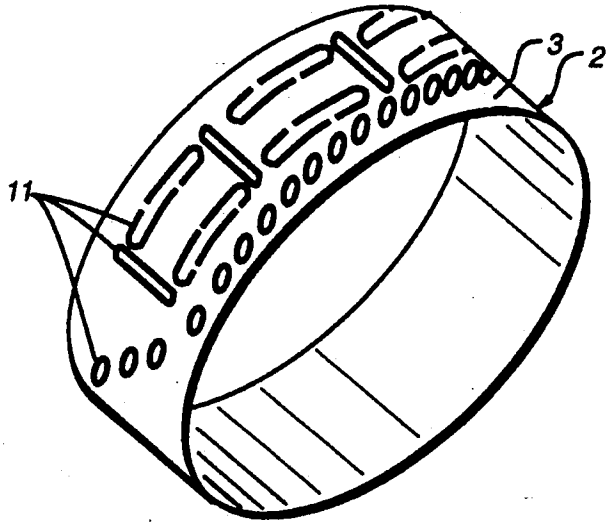


FIG._2

PROCESS FOR CONTINUOUSLY ELECTROFORMING PARTS SUCH AS INKJET ORIFICE PLATES FOR INKJET PRINTERS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to a continuous process for forming parts by precision microfabrication and, more particularly, to a process for fabricating inkjet orifice plates for printheads of inkjet printers.

2. State of the Art

It is known to provide printheads for inkjet printers wherein the printheads each include a substrate, an intermediate barrier layer, and a nozzle plate including an array of nozzle orifices, each of which is paired with a vaporization chamber in the substrate. Also, a complete inkjet printhead includes mean that connect the vaporization cavities to a single ink supply reservoir.

In practice, the print quality of an inkjet printers depends upon the physical characteristics of the nozzles in its printhead. The geometry of a printhead orifice nozzle affects, for instance, the size, trajectory, and speed of ink drop ejection. In addition, the geometry of a printhead orifice nozzle affects the ink supply flow to the associated vaporization chamber and, in some instances, can affect the manner in which ink is ejected from adjacent nozzles.

In practice, nozzle plates for inkjet printheads often are fabricated from nickel in an lithographic electroforming processes. One example of a suitable lithographic electroforming process is described in U.S. Pat. No. 4,773,971, assigned to the Hewlett-Packard Company of Palo Alto, Calif. In the process described in the patent, nickel nozzle plates are formed with a reusable mandrel that includes a conductive material covered with a patterned dielectric layer. To form a nozzle plate, the reusable mandrel is inserted in an electroforming bath so that nickel is electroplated onto the conductive areas of the mandrel.

An article entitled "The ThinkJet Orifice Plate: A Part With Many Functions" by Gary L. Siewell et al. in the Hewlett-Packard Journal, May 1985, pages 33-37, discloses an orifice plate made by a single electroforming step wherein nozzles are formed around pillars of photoresist with carefully controlled overplating. More particularly, the article discloses that a stainless steel mandrel is: (1) deburred, burnished, and cleaned; (2) a layer of photoresist is spun on the surface and patterned to form protected areas for manifolds; (3) the exposed surface is uniformly etched to a specified depth; (4) the resist is removed and the mandrel is burnished and cleaned again; (5) a new coat of photoresist is spun on and patterned to define the barriers and standoffs; and (6) the barriers and standoffs are etched.

Further, the Siewell art discloses that the orifice plate can be made by: (1) laminating the stainless steel mandrel with dry film photoresist; (2) exposing and developing the resist so that circular pads, or pillars, are left for orifices or nozzles; (3) electroplating the mandrel with nickel on the exposed stainless steel areas including the insides of grooves etched into the mandrel to define the barrier walls and standoffs; (4) peeling the plating from the mandrel, the electroplated film being easily removed due to an oxide surface on the stainless steel which causes plated metals to only weakly adhere to the oxide surface; and (5) stripping the photoresist from the nickel foil. According to the article, the nickel foil has openings wherever the resist was on the mandrel. Still further, the article states that the resist is used to define edges of each orifice plate, including break tabs which allows a large number of orifice plates formed on the mandrel to be removed in a single piece, bonded to a mating array of thin-film substrates and separated into individual printheads.

SUMMARY OF THE INVENTION

Generally speaking, the present invention provides a continuous electroforming process and apparatus for manufacturing parts requiring precision micro-fabrication. In a preferred embodiment, the process includes a first step of moving a surface of a mandrel having a reusable pattern thereon through an electroforming bath, a second step of depositing a metal layer on the surface of the mandrel in the shape of the pattern while the mandrel surface moves through the bath, and a third step of separating the metal layer from the mandrel surface after the metal layer has been deposited to a selected thickness.

In practice, the mandrel can take various forms. For instance, the mandrel can be a movable belt. In an alternative embodiment, the mandrel can be a rotatable drum.

When the mandrel is a movable belt, the belt can be made, for instance, of a sheet of polymer material such as polyimide having a metallized thin film such as titanium or chromium/titanium thereon forming the reusable pattern. Alternatively, the belt can comprise a sheet of electrically conductive material having a dielectric material such as silicon carbide, nitride or oxide thereon for defining the reusable pattern.

When the mandrel is a drum, the drum can comprise an electrically conductive material such as stainless steel having a dielectric material thereon such as silicon carbide, nitride or oxide that define the reusable pattern. The electrically conductive material allows an electroplated layer of metal such as nickel to be built up thereon in the shape of the reusable pattern.

Preferably, the reusable pattern is in the shape of a device having details in microns in height, width and depth dimensions. More particularly, the device comprises an orifice plate and the reusable pattern defines the plate's features by photolithography.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be further understood by reference to the following description and attached drawings which illustrate the preferred embodiments. In the drawings:

FIG. 1 shows an apparatus useful for carrying out one embodiment of a process according to the invention; and

FIG. 2 shows a component of the apparatus shown in FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following, there will described a continuous electroforming process for manufacturing parts by precision micro-fabrication. The micro-fabricated parts can include, for example, orifice plates for printers, inkjet orifice plates, and masks for laser processing or for spectrophotometers.

In the micro-fabrication process, the first step comprises moving a surface of a mandrel having a reusable

pattern thereon through an electroforming bath. The second step comprises depositing a metal layer on the surface of the mandrel in the shape of the reusable pattern while the mandrel surface moves through the bath. The third step comprises separating the metal layer from the mandrel surface after the metal layer has deposited to a selected thickness. In practice, the mandrel can take various forms. For instance, in one embodiment, the mandrel is in the form of a movable belt. In another embodiment, the mandrel is in the form of a rotatable drum.

FIG. 1 shows an electroforming apparatus 1 wherein the mandrel 2 is in the form of a moving belt 3. (The belt 3 is shown by itself in FIG. 2.) In the illustrated embodiment, the belt 3 moves through an electroforming bath 4 which includes an anode 5 such as a sacrificial nickel anode. In operation of the electroforming apparatus, current is applied between the anode 5 and the belt 3. As a result, the belt acts as a cathode, and a metal layer 6 is deposited onto it.

In the embodiment shown in FIGS. 1 and 2, belt 3 is an endless belt supported for rotation in, for example, the counterclockwise direction. In this embodiment, belt 3 is supported by driven rollers 7 and 7*a* located outside the bath 4, while guides 8 are immersed in the bath 4. The deposited metal layer 6 is separated from the belt 3 outside the bath 4 at a location adjacent the intersection of a guide 9 and one of the driven rollers 7*a*. The separated metal layer 6*a* is then wound on a reel 10.

With particular reference to the belt 3 in FIG. 2, it should be noted that the belt includes details of a reusable pattern 11 having microfine dimensions. In the embodiment shown, the belt 3 includes a lower section which moves in a rectilinear path and the anode 5 is parallel to the rectilinear path and faces the lower section of the belt.

When the mandrel is a movable belt, it can comprise a sheet of polymer material such as polyimide having a metallized thin film such as titanium or chromium/-titanium thereon forming the reusable pattern. Alternatively, the belt can comprise a sheet of electrically conducive material having a dielectric material such as silicon carbide, nitride or oxide thereon for defining the reusable pattern on the electrically conductive material. Preferably, the belt is about 4 mils thick.

Alternatively, the mandrel can be a drum comprised of an electrically conductive material such as stainless steel or other metals (including copper, brass, and steel coated with electroless nickel) having a dielectric material thereon (such as silicon carbide, nitride or oxide) for defining the pattern on the radially outer surface of the drum.

In the case where the mandrel 2 is belt 3, the metallized thin film can be applied by process such as vacuum deposition. More particularly, in this case, the belt can comprise a layer of titanium on a sheet of polyimide. The polyimide material can be, for instance, "KAPTON" which is a product of DuPont or "UPILEX" which is a product of Ube Company of Japan. Alternatively, the metallized thin film can comprise a first layer of chromium which improves adhesion and a second layer of titanium. As still another alternative, the belt can be a layer of titanium on a polyimide sheet with a layer of dielectric material such as silicon nitride on the titanium layer. The dielectric material can be applied by, for instance, a process such as vacuum deposition.

The belt can be fabricated in a number of ways. For instance, a thin metal film can be metallized on a polyimide substrate. The metallized film is preferably mirror polished to provide the highest quality parts when electroforming the metal layer on the belt. The reusable pattern 11 on the belt 3 can be defined by photolithography so as to provide a photoresist having a shape of the pattern 11 on the thin metal film. The thin metal film is etched such as by chemical etching, dry etching or plasma etching through to the polyimide substrate such that the thin metal film which remains after the etching has the shape of the photoresist. Then, the photoresist is removed to provide the belt 3 with the reusable pattern 11 thereon.

Another way of making the belt is as follows. First, a sheet of polymer material such as polyimide is coated by a process such as by sputter depositing with a layer of electrically conductive material such as titanium or a first layer of chromium and a second layer of titanium over the chromium. Then, the electrically conductive material is coated with a layer of dielectric material such as silicon carbide, nitride or oxide. Then the reusable pattern 11 is defined by photolithography so a to provide a photoresist mask having a shape that defines the reusable pattern 11 on the dielectric layer. The dielectric layer is then etched such as by chemical etching, dry etching or plasma etching through to the electrically conductive material such that the dielectric layer which remains after the etching step has the shape of the photoresist. Then the photoresist is removed thereby providing the belt 3 with the pattern 11 thereon.

The drum can be prepared in a similar manner. In particular, in the case where the drum is of stainless steel, the pattern 11 can be defined on the drum's outer periphery by photolithography. One advantage of this is that the insulating or dielectric material defines the pattern 11.

In the above-described electroforming process, it is preferred that the deposited metal layer 6 is separated from the mandrel 2 outside the bath 4 after the deposited metal layer 6 has a selected thickness. To control the thickness of the deposited metal layer 6, adjustments can be made to the current applied between anode 5 and mandrel 2, or to the speed that the surface of the mandrel 2 moves through the bath 4.

The bath 4 can comprise a nickel-Watts bath, a nickel-sulfamate bath or any other suitable bath. The anode can be a sacrificial anode or the deposited metal layer 6 can be obtained directly from the electrolyte forming the bath. In the case where a nickel-Watts bath is used, the bath can contain nickel chloride, nickel sulfate, boric acid and organic additives such as a leveler, a brightener and a stress reducer.

When the above-described process is used to manufacture inkjet orifice plates, the pattern 11 on the mandrel can be used for forming inkjet orifice plates. Accordingly, the deposited metal layer 6 separated from the mandrel 2 will include a plurality of plates, each having the shape and features of an inkjet orifice plate with the plates being connected together in the form of a continuous sheet. The process can further include a step of bonding the plates to suitable thin-film substrates and a step of separating the bonded plates and substrates into individual printheads.

The foregoing has described the principles, preferred embodiments and modes of operation of the present invention. However, the invention should not be construed as being limited to the particular embodiments discussed. Thus, the above-described embodiments

should be regarded as illustrative rather than restrictive, and it should be appreciated that variations may be made in those embodiments by workers skilled in the art without departing from the scope of present invention as defined by the following claims.

What is claimed is:

1. A continuous electroforming process for forming inkjet orifice plates and similar parts requiring precision micro-fabrication, the process comprising:

a first step of moving a surface of a mandrel having a reusable micro-fabrication pattern thereon through an electroforming bath wherein details of the pattern have microfine dimensions;

a second step of depositing a metal layer on the surface of the mandrel while the surface of the mandrel moves through the electroforming bath until the metal layer is deposited in the pattern on the surface of the mandrel, wherein the metal layer directly contacts the details of the pattern; and

a third step of separating the metal layer from the surface of the mandrel after the metal layer is deposited in the second step.

2. The process of claim 1, wherein the mandrel comprises a moving belt.

3. The process of claim 2, wherein the belt comprises a sheet of electrically conductive material having a dielectric material thereon which defines the pattern.

4. The process of claim 1, wherein the mandrel comprises a rotating drum.

5. The process of claim 1, wherein the drum comprises an electrically conductive material of stainless steel having a dielectric material thereon which defines the pattern.

6. The process of claim 3, wherein the dielectric material is a material selected from the group consisting of silicon nitride, carbide and oxide.

7. The process of claim 1, wherein the thickness of the metal layer deposited in the second step is controlled by adjusting an applied current between the mandrel and an anode in the electroforming bath.

8. The process of claim 1, wherein the thickness of the metal layer deposited in the second step is controlled by adjusting a speed at which the mandrel surface moves through the electroforming bath.

9. The process of claim 1, wherein the metal layer applied in the second step comprises nickel.

10. The process of claim 1, wherein the mandrel comprises a flexible moving belt.

11. The process of claim 1, wherein the mandrel comprises a moving belt having a lower section that follows a rectilinear path through the bath.

12. The process of claim 2, wherein the belt includes a thin film of electrically conductive material having a dielectric material thereon outlining the pattern.

13. A continuous electroforming process for forming inkjet orifice plates and similar parts requiring precision micro-fabrication, the process comprising:

a first step of moving a surface of a mandrel having a reusable pattern thereon through an electroforming bath wherein the mandrel includes a moving belt comprising a sheet of polymer material having a metallized thin film thereon forming the pattern;

a second step of depositing a metal layer on the surface of the mandrel while the surface of the mandrel moves through the electroforming bath until the metal layer is deposited in the pattern on the surface of the mandrel; and

a third step of separating the metal layer from the surface of the mandrel after the metal layer is deposited in the second step.

14. The process of claim 13, wherein the metallized thin film comprises a layer of titanium.

15. The process of claim 13, wherein the metallized thin film comprises a first layer of chromium and a second layer of titanium, the chromium layer being between the sheet of polymer material and the layer of titanium.

16. The process of claim 13, wherein the mandrel includes a thin film of electrically conductive material having a dielectric material thereon outlining the pattern.

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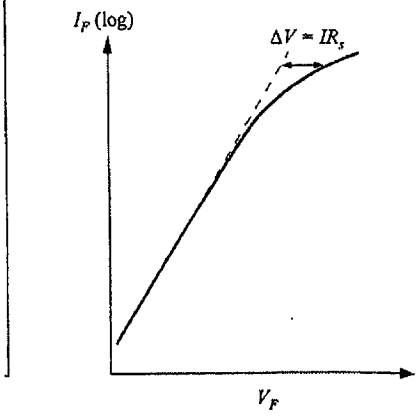
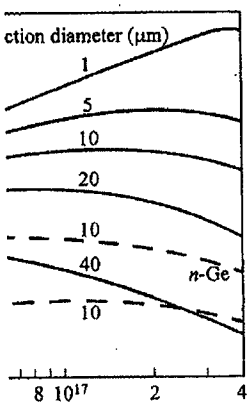


(b)

as a function of applied voltage for Au-Si, f. 80.) (b) Estimate of series resistance from



; doping concentration in the epitaxial layer ers. (After Ref. 80.)

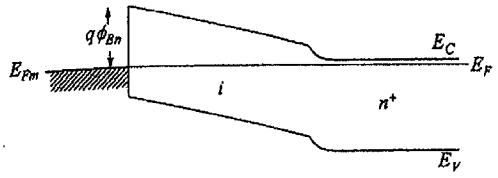


Fig. 38 Band diagram for Mott barrier at zero bias.

larger.[82] The current transport in a Mott barrier is dominated by diffusion, given by Eq. 72, due to the low majority-carrier concentration in the depletion region.

3.6 OHMIC CONTACT

An ohmic contact is defined as a metal-semiconductor contact that has a negligible junction resistance relative to the total resistance of the semiconductor device. A satisfactory ohmic contact should not significantly perturb the device performance and can supply the required current with a voltage drop that is sufficiently small compared with the drop across the active region of the device. The last connection to any semiconductor device is always an on-chip metallic layer. Thus, for every semiconductor device there are at least two metal-semiconductor contacts to form connections. So a good ohmic is a must for every semiconductor device.

The macroscopic parameter—specific contact resistance is defined as the reciprocal of the derivative of the current density with respect to the voltage across the interface. When evaluated at zero bias, this specific contact resistance R_c is an important figure-of-merit for ohmic contacts:[83]

$$R_c \equiv \left(\frac{dJ}{dV}\right)^{-1}_{V=0}. \tag{125}$$

Computer numerical simulation can be performed to get the solution.[83,84] Alternatively, to derive this R_c analytically, the I-V relationships described earlier in the chapter can be used. Again we use the comparison of doping (E_{00}) to temperature (kT) to decide which current mechanism is the dominant one.

For low to moderate doping levels and/or moderately high temperatures, $kT \gg E_{00}$, the standard thermionic-emission expression (Eq. 84) is used to obtain

$$R_c = \frac{k}{A^{**}Tq}\exp\left(\frac{q\phi_{Bn}}{kT}\right) \propto \exp\left(\frac{q\phi_{Bn}}{kT}\right). \tag{126}$$

Since only small applied voltage is relevant, the voltage dependence of the barrier height can be neglected. Equation 126 shows that low barrier height should be used to obtain small R_c.

For higher doping level, $kT \approx E_{oo}$, TFE dominates and R_c is given by[39,85]

$$R_c = \frac{k\sqrt{E_{00}}\cosh(E_{00}/kT)\coth(E_{00}/kT)}{A^{**}Tq\sqrt{\pi q(\phi_{Bn}-\phi_n)}}\exp\left[\frac{q(\phi_{Bn}-\phi_n)}{E_{00}\coth(E_{00}/kT)}+\frac{q\phi_n}{kT}\right]$$
$$\propto \exp\left[\frac{q\phi_{Bn}}{E_{00}\coth(E_{00}/kT)}\right]. \qquad (127)$$

(ϕ_n is negative for degenerate semiconductor.) This type of tunneling occurs at an energy above the conduction band where the product of carrier density and tunneling probability is at a maximum, given by E_m of Eq. 93.

With even higher doping level, $kT \ll E_{oo}$, FE dominates, and the specific contact resistance is given by[39,85]

$$R_c = \frac{k\sin(\pi c_1 kT)}{A^{**}\pi qT}\exp\left(\frac{q\phi_{Bn}}{E_{00}}\right) \propto \exp\left(\frac{q\phi_{Bn}}{E_{00}}\right). \qquad (128)$$

Provided that the barrier height cannot be made very small, a good ohmic contact should operate in this regime of tunneling.

Specific contact resistance is a function of the barrier height (in all regimes), doping concentration (in TFE and FE), and temperature (more sensitive in TE and TFE). Qualitative dependence on these parameters is shown in Fig. 39 for a fixed semiconductor material. The trend and the regimes of operation are also indicated in the figure. In TE, R_c is independent of doping concentration and dependent only on the barrier height ϕ_B. In the other extreme of FE, in addition to ϕ_B, R_c has a dependence of $\propto \exp(N^{-1/2})$. The results of calculated specific contact resistance on silicon are given in Fig. 40.

It is quite obvious that to obtain low values of R_c, high doping concentration, low barrier height, or both must be used. And these are exactly the approaches used for all

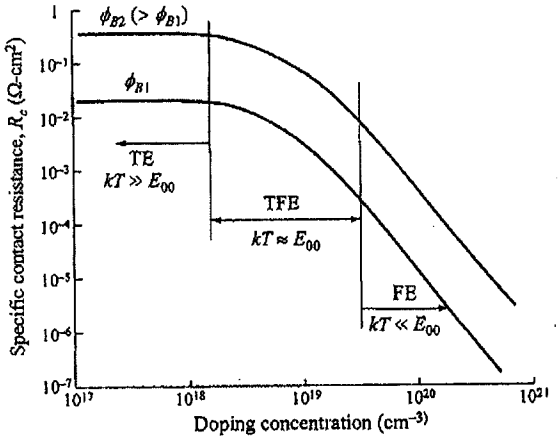


Fig. 39 Dependence of specific contact resistance on doping concentration (and E_{00}), barrier height, and temperature. Regimes of TE, TFE, and FE are indicated.

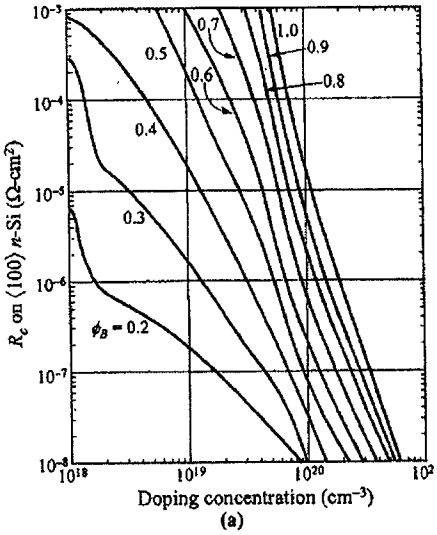


Fig. 40 Calculated specific contact resistanc faces for various barrier heights (in eV) at roo

ohmic contacts. On wide-gap semiconduc tacts. A metal does not generally exist with barrier. In such cases, the general techniqu establishment of a more heavily doped su to add a heterojunction with a layer of sn doping of the same type. For GaAs and various technologies have been develope contact materials on common semiconduc

As devices are miniaturized for advan density usually increases. This demands n smaller contact area. The challenge of f increasing with device miniaturization. Th

$$R = \frac{R}{A}$$

However, this expression is valid only fo area. We mention here two practical condi are important. For a small contact of r spreading resistance in series with the ohn

$$R_{sp} = \frac{\rho}{2\pi r}$$ ta

$$\exp\left[\frac{q(\phi_{Bn}-\phi_n)}{E_{00}\coth(E_{00}/kT)}+\frac{q\phi_n}{kT}\right]$$

(127)

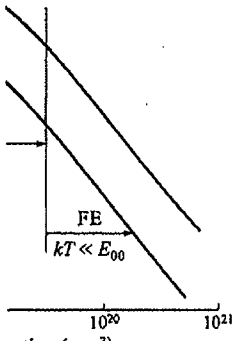
) This type of tunneling occurs at an oduct of carrier density and tunneling]. 93.
E dominates, and the specific contact

$$\propto \exp\left(\frac{q\phi_{Bn}}{E_{00}}\right). \tag{128}$$

de very small, a good ohmic contact

f the barrier height (in all regimes), nperature (more sensitive in TE and eters is shown in Fig. 39 for a fixed nes of operation are also indicated in concentration and dependent only on 'E, in addition to ϕ_B, R_c has a depen- specific contact resistance on silicon

of R_c, high doping concentration, low ıre exactly the approaches used for all



n doping concentration (and E_{00}), barrier E are indicated.

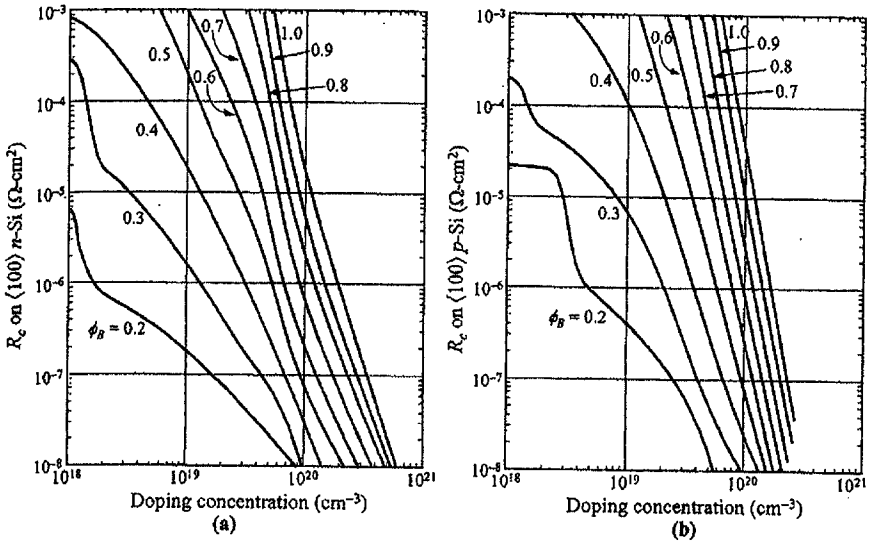


Fig. 40 Calculated specific contact resistance R_c on (a) n-type and (b) p-type ⟨100⟩ Si surfaces for various barrier heights (in eV) at room temperature. (After Ref. 86)

ohmic contacts. On wide-gap semiconductors it is difficult to make good ohmic contacts. A metal does not generally exist with a low enough work function to yield a low barrier. In such cases, the general technique for making an ohmic contact involves the establishment of a more heavily doped surface layer. Another common technique is to add a heterojunction with a layer of small bandgap material and with high-level doping of the same type. For GaAs and other III-V compound semiconductors, various technologies have been developed for the ohmic contacts.[87] A summary of contact materials on common semiconductors is listed in Table 5.

As devices are miniaturized for advanced integrated circuits, the device current density usually increases. This demands not only smaller ohmic resistance but also a smaller contact area. The challenge of fabricating good ohmic contacts has been increasing with device miniaturization. The total contact resistance is given by

$$R = \frac{R_c}{A}. \tag{129}$$

However, this expression is valid only for uniform current density across the whole area. We mention here two practical conditions that additional resistance components are important. For a small contact of radius r as shown in Fig. 41a, there is a spreading resistance in series with the ohmic contact given by[89]

$$R_{sp} = \frac{\rho}{2\pi r}\tan^{-1}\left(\frac{2h}{r}\right). \tag{130}$$

Table 5 Metal Ohmic Contacts for Various Semiconductors (After Ref. 88)

Semiconductor	Metal	Semiconductor	Metal
n-Ge	Ag-Al-Sb, Al, Al-Au-P, Au, Bi, Sb, Sn, Pb-Sn	*p*-Ge	Ag, Al, Au, Cu, Ga, Ga-In, In, Al-Pd, Ni, Pt, Sn
n-Si	Ag, Al, Al-Au, Ni, Sn, In, Ge-Sn, Sb, Au-Sb, Ti, TiN	*p*-Si	Ag, Al, Al-Au, Au, Ni, Pt, Sn, In, Pb, Ga, Ge, Ti, TiN
n-GaAs	Au(.88)Ge(.12)-Ni, Ag-Sn, Ag(.95)In(.05)-Ge	*p*-GaAs	Au(.84)Zn(.16), Ag-In-Zn, Ag-Zn
n-GaP	Ag-Te-Ni, Al, Au-Si, Au-Sn, In-Sn	*p*-GaP	Au-In, Au-Zn, Ga, In-Zn, Zn, Ag-Zn
n-GaAsP	Au-Sn	*p*-GaAsP	Au-Zn
n-GaAlAs	Au-Ge-Ni	*p*-GaAlAs	Au-Zn
n-InAs	Au-Ge, Au-Sn-Ni, Sn	*p*-InAs	Al
n-InGaAs	Au-Ge, Ni	*p*-InGaAs	Au-Zn, Ni
n-InP	Au-Ge, In, Ni, Sn		
n-InSb	Au-Sn, Au-In, Ni, Sn	*p*-InSb	Au-Ge
n-CdS	Ag, Al, Au, Au-In, Ga, In, Ga-In		
n-CdTe	In	*p*-CdTe	Au, In-Ni, Indalloy 13, Pt, Rh
n-ZnSe	In, In-Ga, Pt, InHg		
n-SiC	W	*p*-SiC	Al-Si, Si, Ni

This component approaches the bulk resistance of $\rho h/A$ for large r/h ratios. In cases where the contact is made on a horizontal diffusion layer (Fig. 41b, as in the case of a MOSFET), the total resistance between point X (leading edge of the contact) and the metal contact is given by[90]

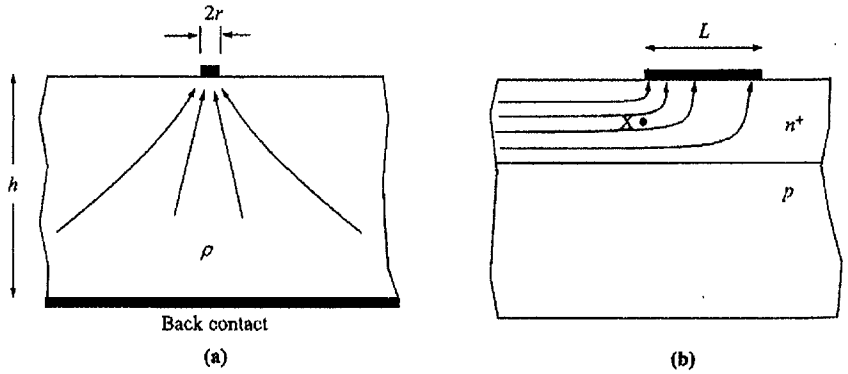


Fig. 41 (a) Current pattern for a small contact when $r \ll h$. r is the radius of the contact. (b) Current pattern for a contact to a horizontal diffusion sheet. If the sheet resistance of the diffusion layer is high, current is forced toward the leading edge of the contact.

where $R_\square$ is the sheet resi
account nonuniform curre
tributions due to the sheet
$R_\square \to 0$, Eq. 131 reduces to

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)onductors (After Ref. 88)

emiconductor	Metal
-Ge	Ag, Al, Au, Cu, Ga, Ga-In, In, Al-Pd, Ni, Pt, Sn
-Si	Ag, Al, Al-Au, Au, Ni, Pt, Sn, In, Pb, Ga, Ge, Ti, TiN
-GaAs	Au(.84)Zn(.16), Ag-In-Zn, Ag-Zn
-GaP	Au-In, Au-Zn, Ga, In-Zn, Zn, Ag-Zn
-GaAsP	Au-Zn
-GaAlAs	Au-Zn
-InAs	Al
-InGaAs	Au-Zn, Ni
-InSb	Au-Ge
-CdTe	Au, In-Ni, Indalloy 13, Pt, Rh
-SiC	Al-Si, Si, Ni

ice of ios. In cases the case of ntact) and

$$R = \frac{\sqrt{R_\square R_c}}{W} \coth\left(L\sqrt{\frac{R_\square}{R_c}}\right) \tag{131}$$

where $R_\square$ is the sheet resistance ($\Omega/\square$) of the diffusion layer. This equation takes into account nonuniform current density through the contact (current crowding) and contributions due to the sheet resistance itself. It can also be shown that in the limit of $R_\square \to 0$, Eq. 131 reduces to Eq. 129.

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X. RELATED PROCEEDINGS APPENDIX

None.